Bi-CMOS LSI

LV8729V — PWM Constant-Current Control Stepping Motor Driver

Overview

The LV8729V is a PWM current-controlled micro step bipolar stepping motor driver.
This driver can do eight ways of micro step resolution of 1/128 step from Full step, and can drive simply by the CLK input.

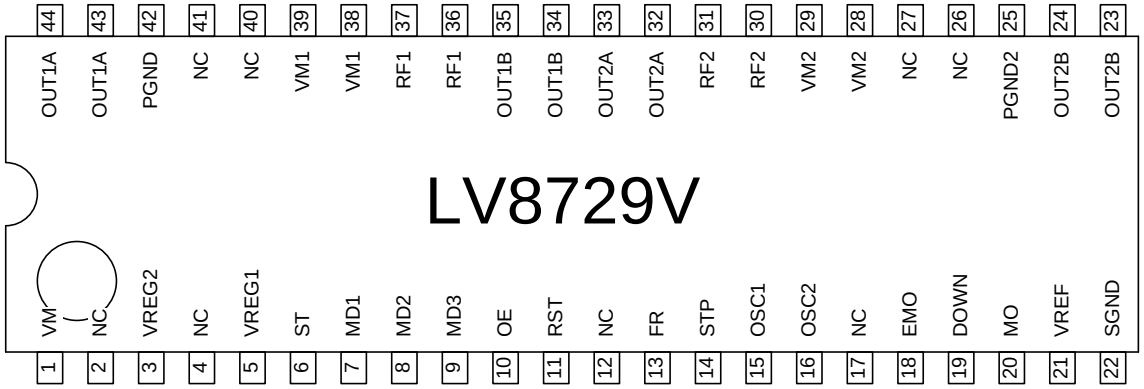
Features

- Single-channel PWM current control stepping motor driver.
- BiCDMOS process IC.
- Output on-resistance (upper side : 0.35Ω ; lower side : 0.3Ω ; total of upper and lower : 0.65Ω ; Ta = 25°C, I_O = 1.8A)
- Full, Half, Quarter, 1/8, 1/16, 1/32, 1/64, 1/128 Step are selectable.
- Advance the excitation step with the only step signal input.
- Available forward reverse control.
- Over current protection circuit.
- Thermal shutdown circuit.
- Input pull down resistance.
- With reset pin and enable pin.

Typical Applications

- Security camera
- Projector
- Stage Lighting
- Industrial Printer

Pin Assignment

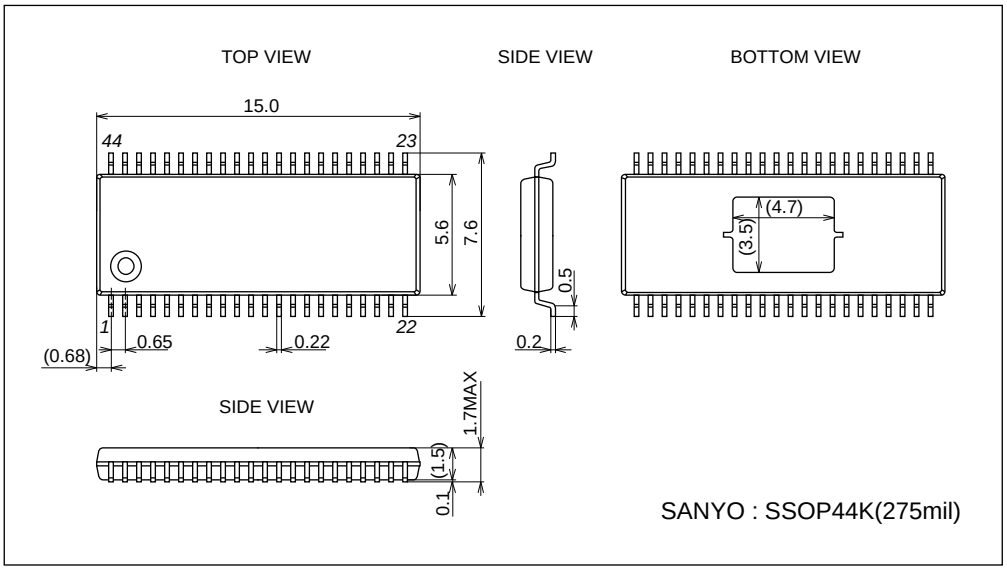


Top view

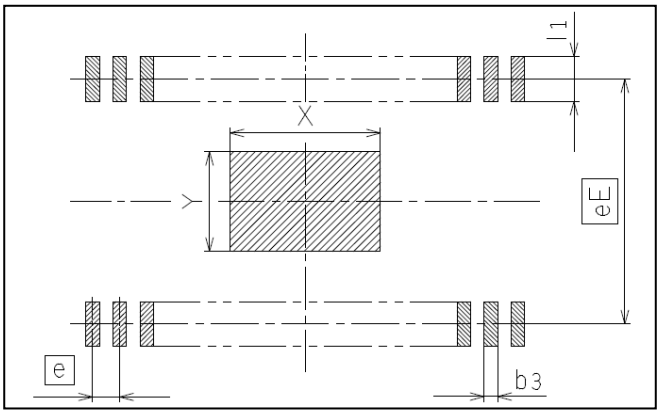
Package Dimensions

unit : mm (typ)

3333



Mounting Pad Sketch

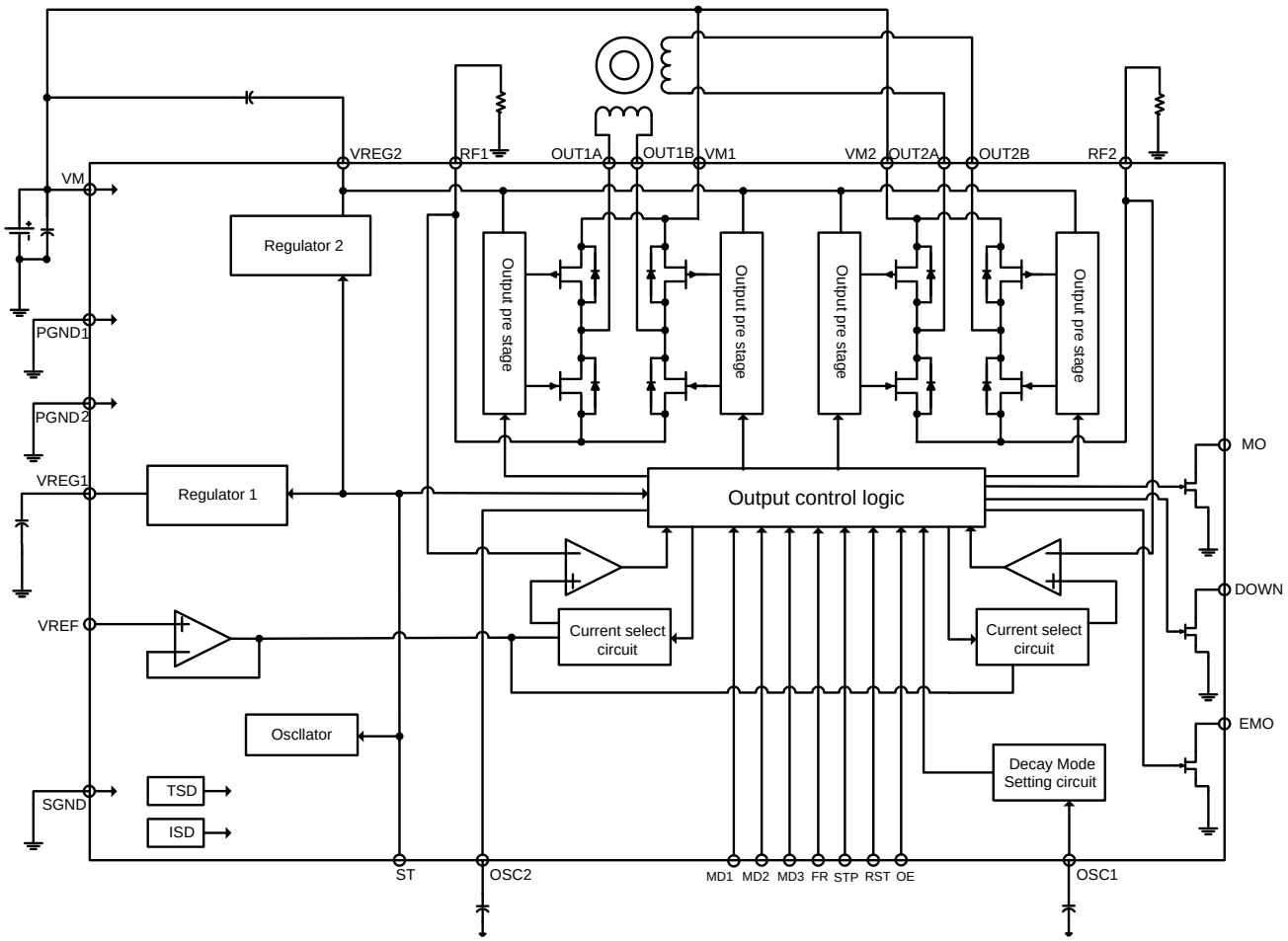


Reference symbol	SSOP44K(275mil)
eE	7.00
e	0.65
b3	0.32
l1	1.00
X	(4.7)
Y	(3.5)

(Unit:mm)

Caution: The package dimension is a reference value, which is not a guaranteed value.

Block Diagram



Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	VM max		36	V
Maximum output peak current	I_O max		1.8	A
Maximum logic input voltage	V_{IN} max		6	V
Maximum VREF input voltage	VREF max		6	V
Maximum MO input voltage	V_{MO} max		6	V
Maximum DOWN input voltage	V_{DOWN} max		6	V
Allowable power dissipation	Pd max	*	3.85	W
Operating temperature	Topr		-30 to +85	°C
Storage temperature	Tstg		-55 to +150	°C

* Specified circuit board : 90.0mm×90.0mm×1.6mm, glass epoxy 2-layer board, with backside mounting.

Allowable Operating Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage range	VM		9 to 32	V
Logic input voltage	V_{IN}		0 to 5	V
VREF input voltage range	VREF		0 to 3	V

Electrical Characteristics at Ta = 25°C, VM = 24V, VREF = 1.5V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Standby mode current drain	I_Mst	ST = “L”		70	100	μA
Current drain	IM	ST = “H”, OE = “H”, no load		3.3	4.6	mA
Thermal shutdown temperature	TSD	Design guarantee	150	180	200	°C
Thermal hysteresis width	ΔTSD	Design guarantee		40		°C
Logic pin input current	I_{IN}L	V_{IN} = 0.8V	3	8	15	μA
	I_{IN}H	V_{IN} = 5V	30	50	70	μA
Logic high-level input voltage	V_{IN}H		2.0			V
Logic low-level input voltage	V_{IN}L				0.8	V
Chopping frequency	Fch	Cosc1 = 100pF	70	100	130	kHz
OSC1 pin charge/discharge current	Iosc1		7	10	13	μA
Chopping oscillation circuit threshold voltage	Vtup1		0.8	1	1.2	V
	Vtdown1		0.3	0.5	0.7	V
VREF pin input voltage	Iref	VREF = 1.5V	-0.5			μA
DOWN output residual voltage	V_O1DOWN	Idown = 1mA		40	100	mV
MO pin residual voltage	V_O1MO	Imo = 1mA		40	100	mV
Hold current switching frequency	Fdown	Cosc2 = 1500pF	1.12	1.6	2.08	Hz
Hold current switching frequency threshold voltage	Vtup2		0.8	1	1.2	V
	Vtdown2		0.3	0.5	0.7	V
VREG1 output voltage	Vreg1		4.7	5	5.3	V
VREG2 output voltage	Vreg2	$V_{M=24V}$	18	19	20	V
Output on-resistance	Ronu	I_O = 1.8A, high-side ON resistance		0.35	0.455	Ω
	Rond	I_O = 1.8A, low-side ON resistance		0.3	0.39	Ω
Output leakage current	$I_O$leak	V_M = 36V			50	μA
Diode forward voltage	VD	I_D = -1.8A		1	1.4	V
Current setting reference voltage	VRF	VREF = 1.5V, Current ratio 100%	0.285	0.3	0.315	V

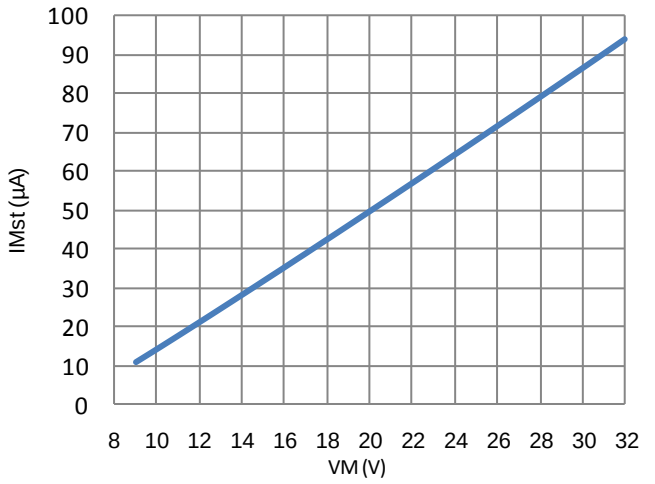


Figure1 Standby Mode Current Drain vs VM Voltage

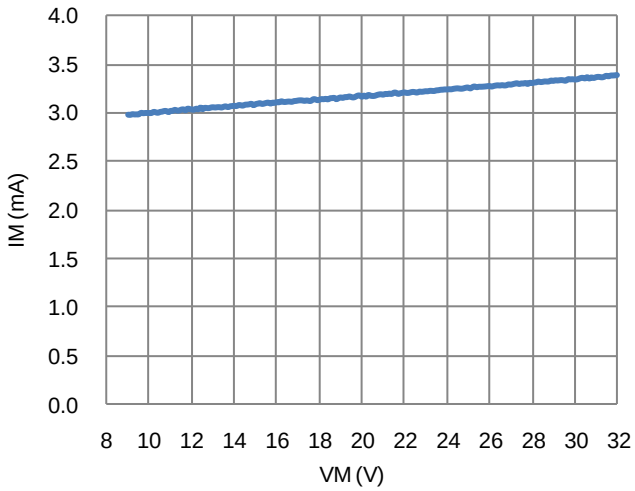


Figure2 Current Drain vs VM Voltage

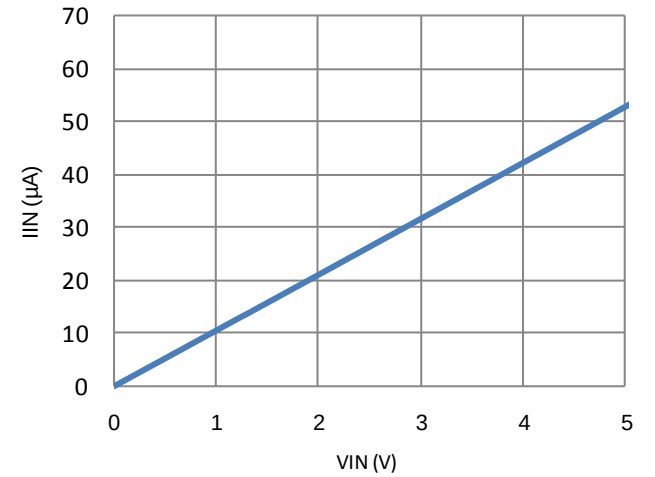


Figure3 Logic Pin Input Current vs VIN Voltage (VM=24V)

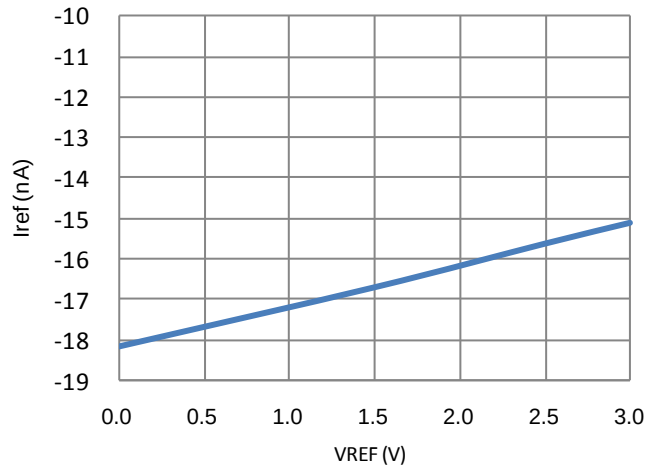


Figure4 VREF Pin Input Current vs VREF Voltage (VM=24V)

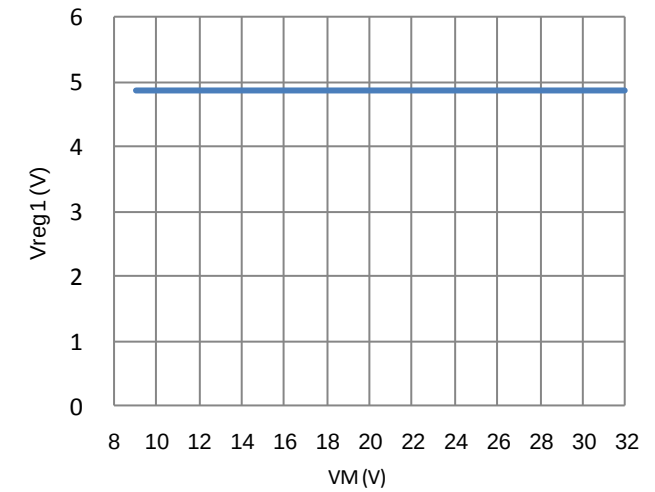


Figure5 VREG1 Output Voltage vs VM Voltage

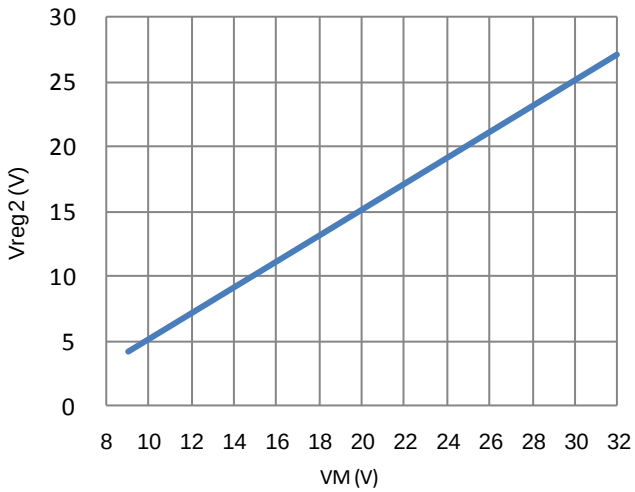


Figure6 VREG2 Output Voltage vs VM Voltage

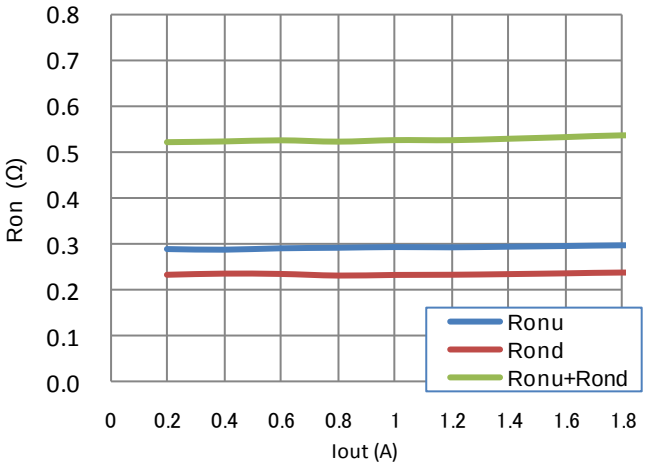


Figure7 Output on Resistance vs Output Current (VM=24V)

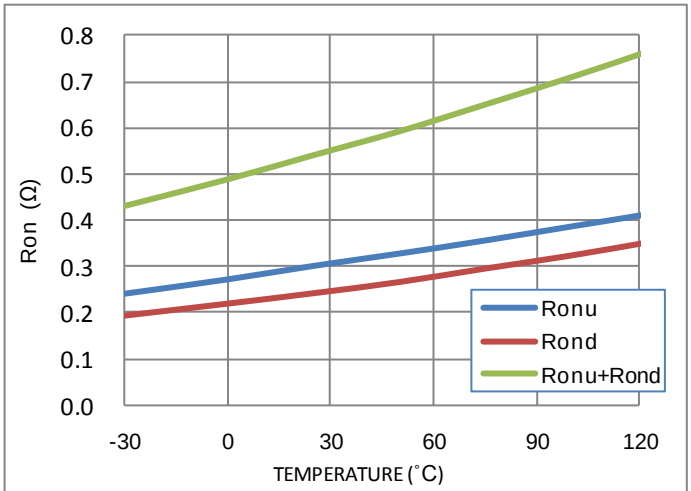


Figure8 Output on Resistance vs Temperature (VM=24V)

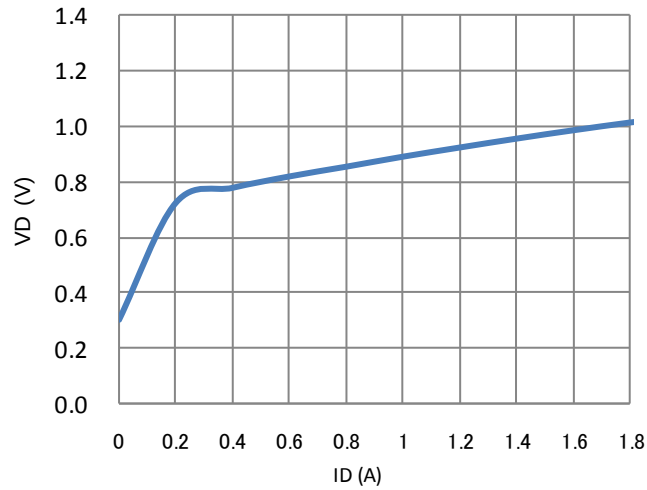


Figure9 Diode Foward Voltage vs Diode Current

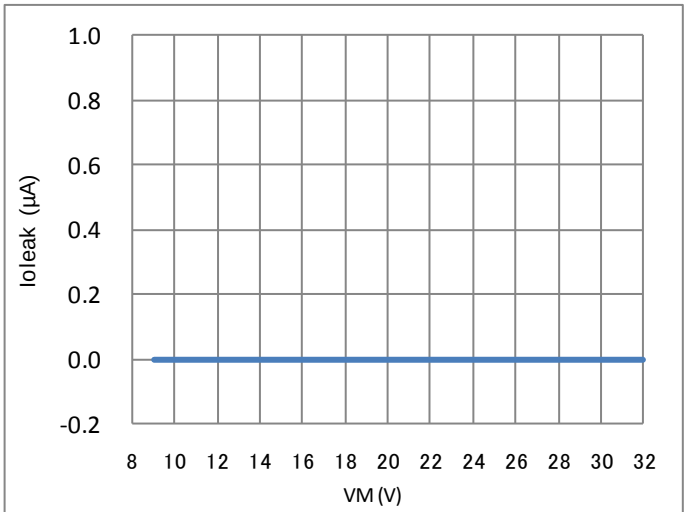
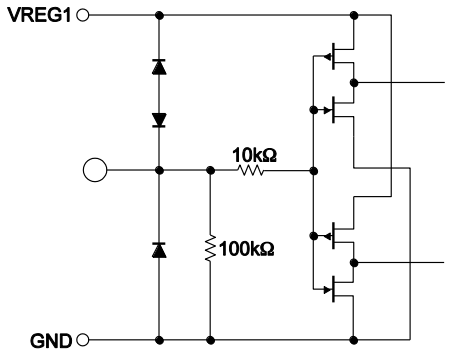
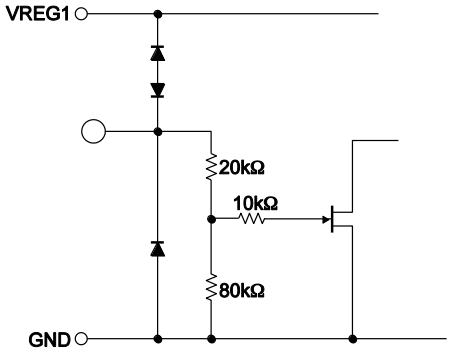
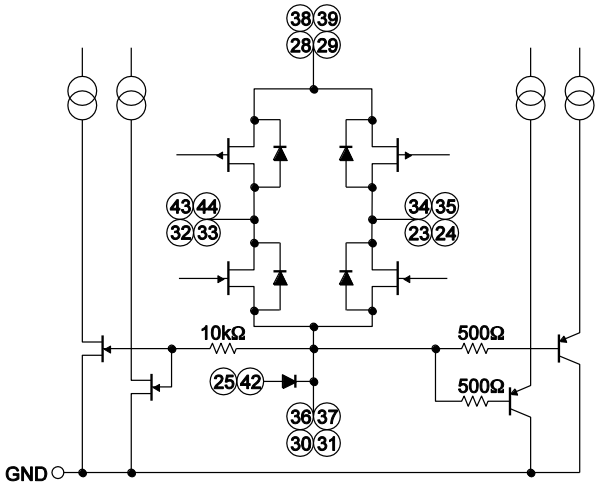
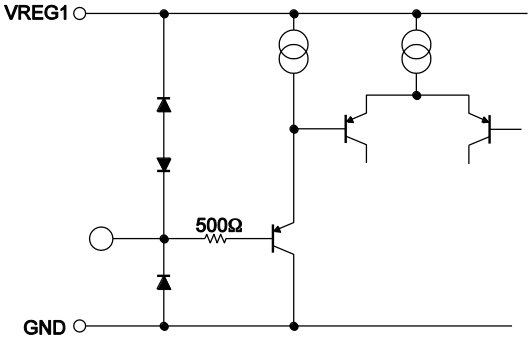


Figure10 Output Leakage Current vs VM Voltage

Pin Functions

Pin No.	Pin Name	Pin Function	Equivalent Circuit
7 8 9 10 11 13 14	MD1 MD2 MD3 OE RST FR STP	Excitation mode switching pin Excitation mode switching pin Excitation mode switching pin Output enable signal input pin Reset signal input pin Forward / Reverse signal input pin Step clock pulse signal input pin	
6	ST	Chip enable pin.	
23, 24 25 28, 29 30, 31 32, 33 34, 35 36, 37 38, 39 42 43, 44	OUT2B PGND2 V_M2 RF2 OUT2A OUT1B RF1 V_M1 PGND1 OUT1A	Channel 2 OUTB output pin. Channel 2 Power system ground Channel 2 motor power supply connection pin. Channel 2 current-sense resistor connection pin. Channel 2 OUTA output pin. Channel 1 OUTB output pin. Channel 1 current-sense resistor connection pin. Channel 1 motor power supply pin. Channel 1 Power system ground Channel 1 OUTA output pin.	
21	VREF	Constant-current control reference voltage input pin.	

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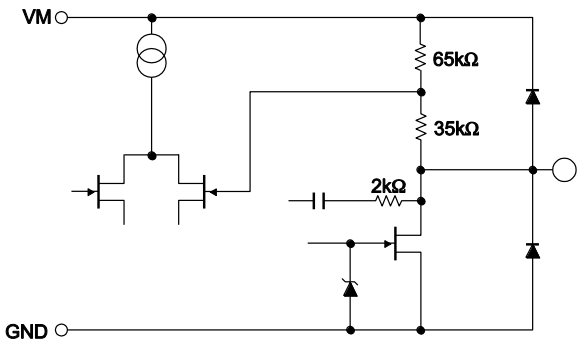
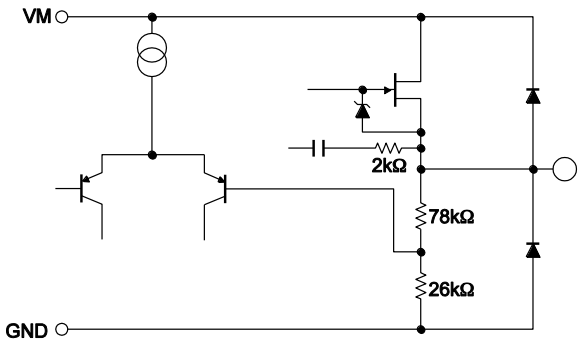
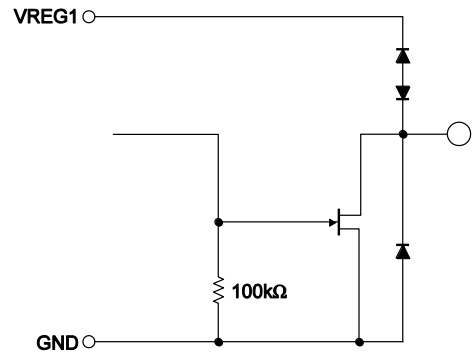
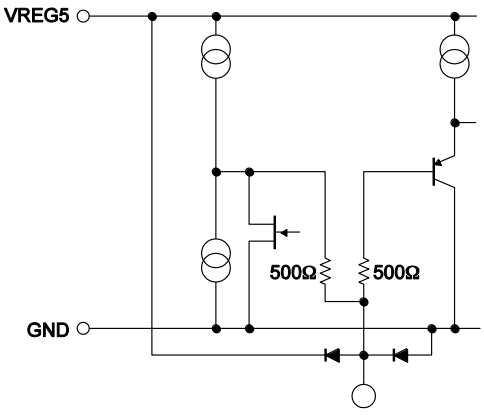
Pin No.	Pin Name	Pin Function	Equivalent Circuit
3	VREG2	Internal regulator capacitor connection pin.	
5	VREG1	Internal regulator capacitor connection pin.	
18 19 20	EMO DOWN MO	Over-current detection alarm output pin. Holding current output pin. Position detecting monitor pin.	
15 16	OSC1 OSC2	Copping frequency setting capacitor connection pin. Holding current detection time setting capacitor connection pin.	

Reference describing operation

(1) Stand-by function

When ST pin is at low levels, the IC enters stand-by mode, all logic is reset and output is turned OFF.
When ST pin is at high levels, the stand-by mode is released.

(2) STEP pin function

STEP input advances electrical angle at every rising edge (advances step by step) .

Input		Operating mode
ST	STP	
Low	*	Standby mode
High		Excitation step proceeds
High		Excitation step is kept

STEP input MIN pulse width (common in H/L): 500ns (MAX input frequency: 1MHz)
However, constant current control is performed by PWM during chopping period, which is set by the capacitor connected between OSC1 and GND. You need to perform chopping more than once per step. For this reason, for the actual STEP frequency, you need to take chopping frequency and chopping count into consideration.
For example, if chopping frequency is 50kHz (20μs) and chopping is performed twice per step, the maximum STEP frequency is obtained as follows: f＝1/(20μs×2) = 25kHz.

(3) Input timing

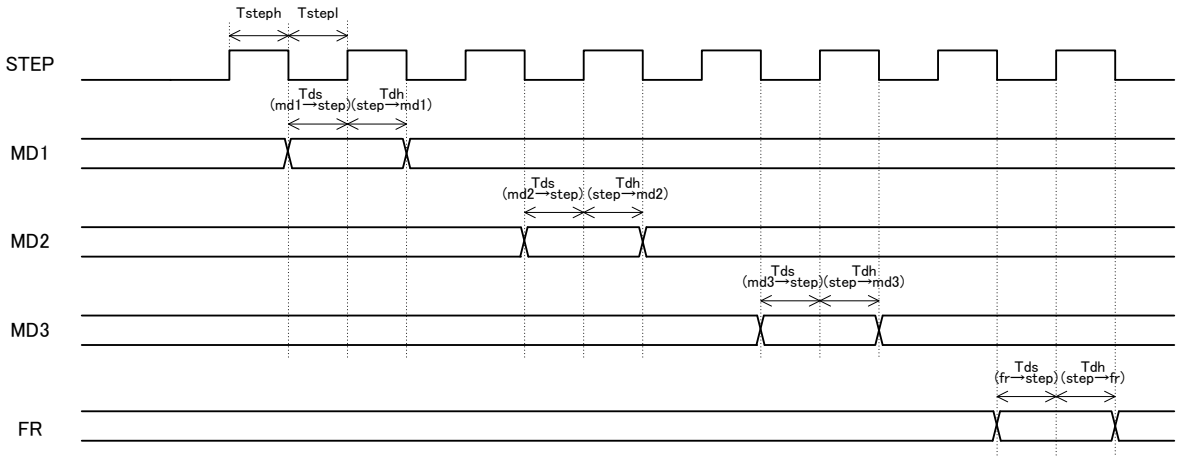


Figure 11. Input timing chart

TstepH/TstepL : Clock H/L pulse width (min 500ns)
Tds : Data set-up time (min 500ns)
Tdh : Data hold time (min 500ns)

(4) Excitation setting method

Set the micro step resolution setting as shown in the following table by setting MD1 pin, MD2 pin and MD3 pin.

Input			Micro step resolution	Excitation mode	Initial position	
MD3	MD2	MD1			1ch current	2ch current
Low	Low	Low	Full Step	2-phase	100%	-100%
Low	Low	High	Half Step	1-2 phase	100%	0%
Low	High	Low	Quarter Step	W1-2 phase	100%	0%
Low	High	High	1/8 Step	2W1-2 phase	100%	0%
High	Low	Low	1/16 Step	4W1-2 phase	100%	0%
High	Low	High	1/32 Step	8W1-2 phase	100%	0%
High	High	Low	1/64 Step	16W1-2 phase	100%	0%
High	High	High	1/128 Step	32W1-2 phase	100%	0%

The initial position is also the default state at start-up and excitation position at counter-reset in each Micro step resolution.

(5) Position detection monitoring function

The MO position detection monitoring pin is of an open drain type.
When the excitation position is in the initial position, the MO output is placed in the ON state.
(Refer to "Examples of current waveforms in each of the excitation modes.")

(6) Output current setting

Output current is set shown below by the VREF pin (applied voltage) and a resistance value between RF1(2) pin and GND.

I_{OUT} = (VREF / 5) / RF1 (2) resistance

* The setting value above is a 100% output current in each micro step resolution.

(Example) When VREF = 1.1V and RF1 (2) resistance is 0.22Ω, the setting is shown below.

I_{OUT} = (1.1V / 5) / 0.22Ω = 1.0A

If VREF is open or the setting is out of the recommendation operating range, output current will increase and you cannot set constant current under normal condition. Hence, make sure that VREF is set in accordance with the specification.
However, if current control is not performed (if the IC is used without saturation drive or current limit) make sure that the setting is as follows: VREF=5V or VREF=VREG1

(7) Output enable function

When the OE pin is set Low, the output is forced OFF and goes to high impedance. However, the internal logic circuits are operating, so the excitation position proceeds when the STP is input. Therefore, when OE pin is returned to High, the output level conforms to the excitation position proceeded by the STP input.

OE	Operating mode
High	Output ON
Low	Output OFF

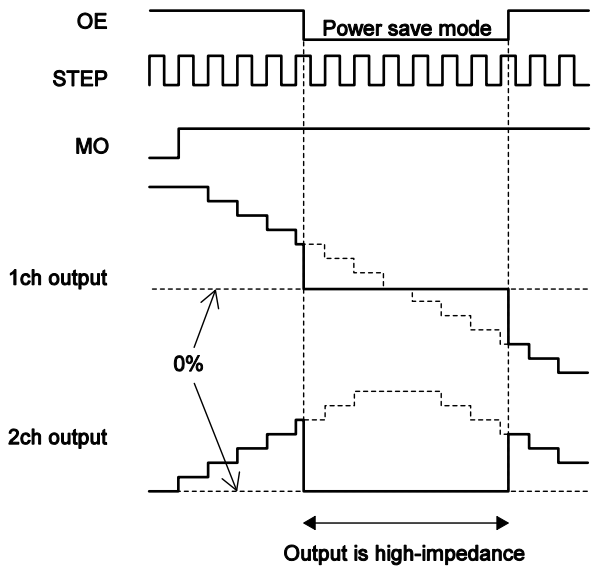


Figure 12. Output enable function timing chart

(8) Reset function

When the RST pin is set Low, the output goes to initial mode and excitation position is fixed in the initial position for STP pin and FR pin input. MO pin outputs at low levels at the initial position. (Open drain connection)

RST	Operating mode
High	Normal operation
Low	Reset state

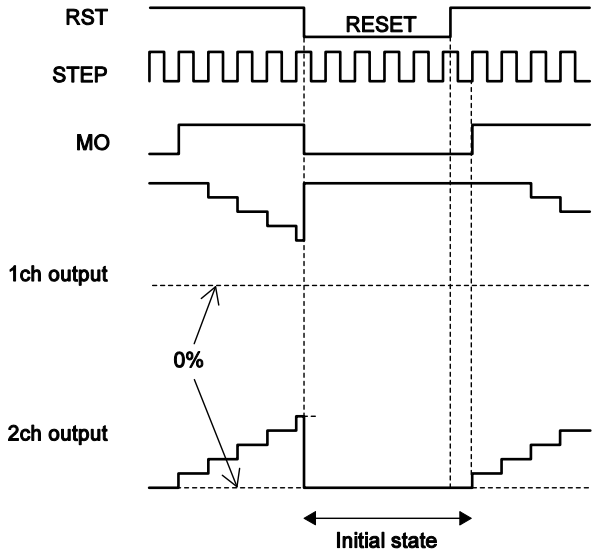


Figure 13. Reset function timing chart

(9) Forward / reverse switching function

FR	Operating mode
Low	Clockwise (CW)
High	Counter-clockwise (CCW)

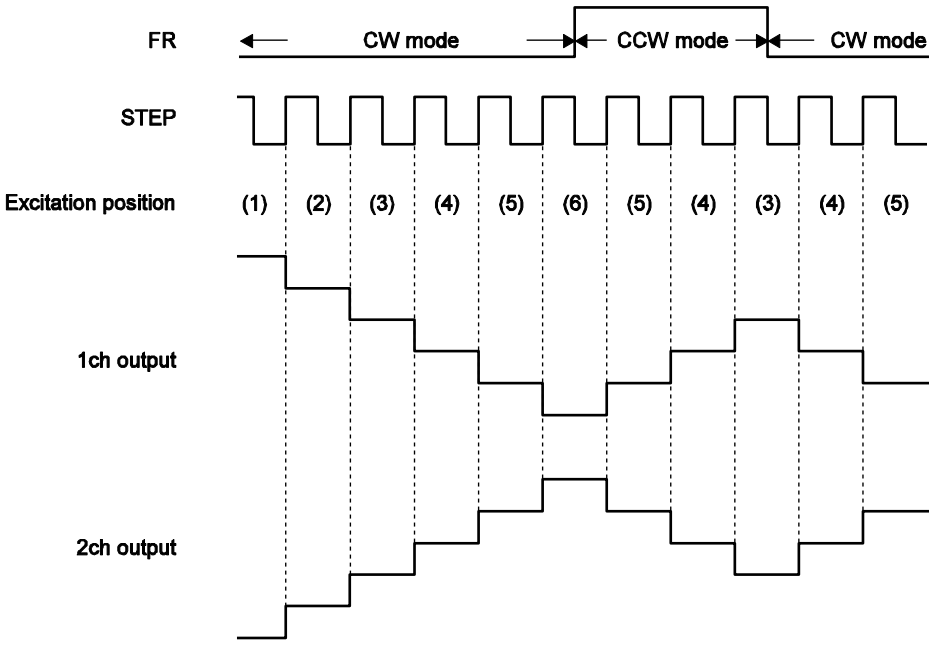


Figure 14.Forward/Reverse switching function timing chart

The internal D/A converter proceeds by a bit on the rising edge of the step signal input to the STP pin. In addition, CW and CCW mode are switched by FR pin setting.

In CW mode, the channel 2 current phase is delayed by 90° relative to the channel 1 current.

In CCW mode, the channel 2 current phase is advanced by 90° relative to the channel 1 current.

(10) EMO, DOWN output pin

The output pin is open -drain connection. When it becomes prescribed, it turns on, and each pin outputs the Low level.

Pin state	EMO	DOWN
Low	At detection of over-current	Holding current state
OFF	Normal state	Normal state

(11) Chopping frequency setting function

Chopping frequency is set as shown below by a capacitor between OSC1 pin and GND.

$$Fcp = 1 / (Cosc1 / 10 \times 10^{-6}) \text{ (Hz)}$$

(Example) When Cosc1 = 180pF, the chopping frequency is shown below.

$$Fcp = 1 / (180 \times 10^{-12} / 10 \times 10^{-6}) = 55.5\text{(kHz)}$$

The higher the chopping frequency is, the greater the output switching loss becomes. As a result, heat generation issue arises.

The lower the chopping frequency is, the lesser the heat generation becomes. However, current ripple occurs.

Since noise increases when switching of chopping takes place, you need to adjust frequency with the influence to the other devices into consideration. The frequency range should be between 40kHz and 125kHz.

(12) Open-drain pin for switching holding current

The output pin is an open-drain connection.

This pin is turned ON when no rising edge of STP between the input signals while a period determined by a capacitor between OSC2 and GND, and outputs at low levels.

The open-drain output in once turned ON, is turned OFF at the next rising edge of STP.

Holding current switching time (Tdown) is set as shown below by a capacitor between OSC2 pin and GND.

$$Tdown = Cosc2 \times 0.4 \times 10^{9} \text{ (s)}$$

(Example) When Cosc2 = 1500pF, the holding current switching time is shown below.

$$Tdown = 1500\text{pF} \times 0.4 \times 10^{9} = 0.6 \text{ (s)}$$

(13) Output current vector locus (one step is normalized to 90 degrees)

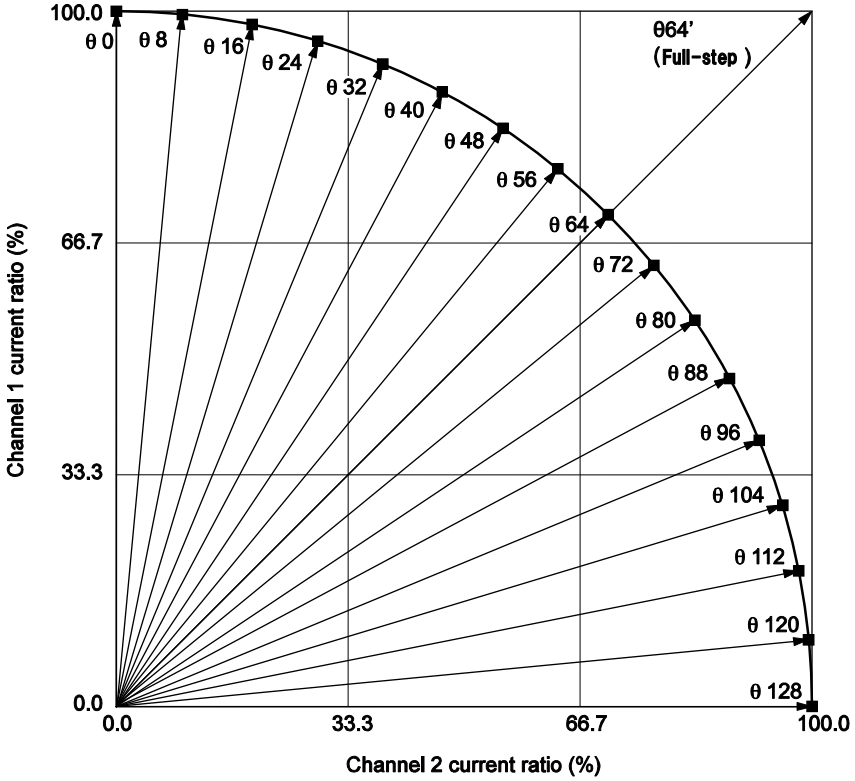


Figure 15.Output current vector

Current setting ratio in each micro step resolution

STEP	1/128 (%)		1/64 (%)		1/32 (%)		1/16 (%)		1/8 (%)		Quarter (%)		Half (%)		Full (%)	
	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch
θ0	100	0	100	0	100	0	100	0	100	0	100	0	100	0		
θ1	100	1														
θ2	100	2	100	2												
θ3	100	4														
θ4	100	5	100	5	100	5										
θ5	100	6														
θ6	100	7	100	7												
θ7	100	9														
θ8	100	10	100	10	100	10	100	10								
θ9	99	11														
θ10	99	12	99	12												
θ11	99	13														
θ12	99	15	99	15	99	15										
θ13	99	16														
θ14	99	17	99	17												
θ15	98	18														
θ16	98	20	98	20	98	20	98	20	98	20						
θ17	98	21														
θ18	98	22	98	22												
θ19	97	23														
θ20	97	24	97	24	97	24										
θ21	97	25														
θ22	96	27	96	27												
θ23	96	28														
θ24	96	29	96	29	96	29	96	29								
θ25	95	30														

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STEP	1/128 (%)		1/64 (%)		1/32 (%)		1/16 (%)		1/8 (%)		Quarter (%)		Half (%)		Full (%)	
	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch
026	95	31	95	31												
027	95	33														
028	94	34	94	34	94	34										
029	94	35														
030	93	36	93	36												
031	93	37														
032	92	38	92	38	92	38	92	38	92	38	92	38				
033	92	39														
034	91	41	91	41												
035	91	42														
036	90	43	90	43	90	43										
037	90	44														
038	89	45	89	45												
039	89	46														
040	88	47	88	47	88	47	88	47								
041	88	48														
042	87	49	87	49												
043	86	50														
044	86	51	86	51	86	51										
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046	84	53	84	53												
047	84	55														
048	83	56	83	56	83	56	83	56	83	56						
049	82	57														
050	82	58	82	58												
051	81	59														
052	80	60	80	60	80	60										
053	80	61														
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055	78	62														
056	77	63	77	63	77	63	77	63								
057	77	64														
058	76	65	76	65												
059	75	66														
060	74	67	74	67	74	67										
061	73	68														
062	72	69	72	69												
063	72	70														
064	71	71	71	71	71	71	71	71	71	71	71	71	71	71	100	100
065	70	72														
066	69	72	69	72												
067	68	73														
068	67	74	67	74	67	74										
069	66	75														
070	65	76	65	76												
071	64	77														
072	63	77	63	77	63	77	63	77								
073	62	78														
074	62	79	62	79												
075	61	80														
076	60	80	60	80	60	80										
077	59	81														
078	58	82	58	82												
079	57	82														
080	56	83	56	83	56	83	56	83	56	83						
081	55	84														
082	53	84	53	84												
083	52	85														
084	51	86	51	86	51	86										
085	50	86														
086	49	87	49	87												
087	48	88														
088	47	88	47	88	47	88	47	88								
089	46	89														
090	45	89	45	89												

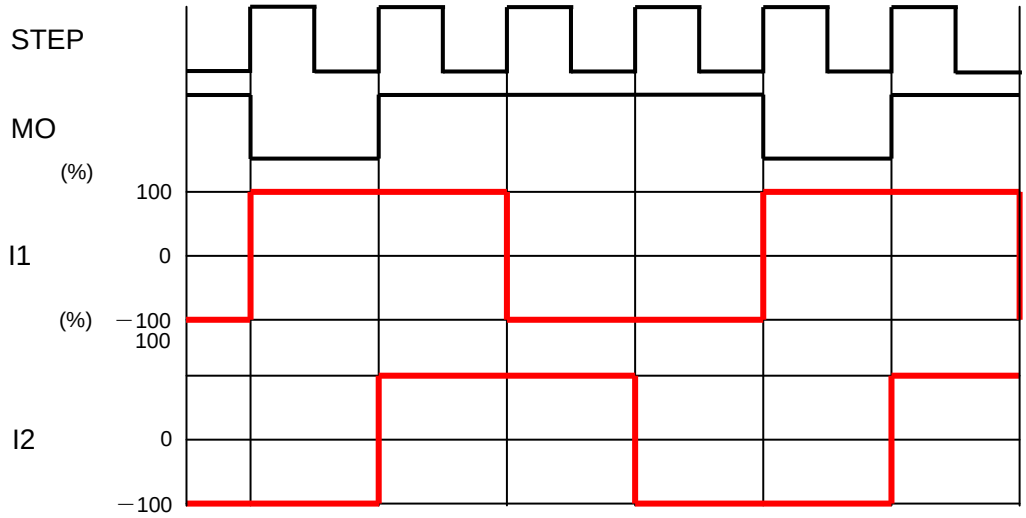
Continued on next page.

Continued from preceding page.

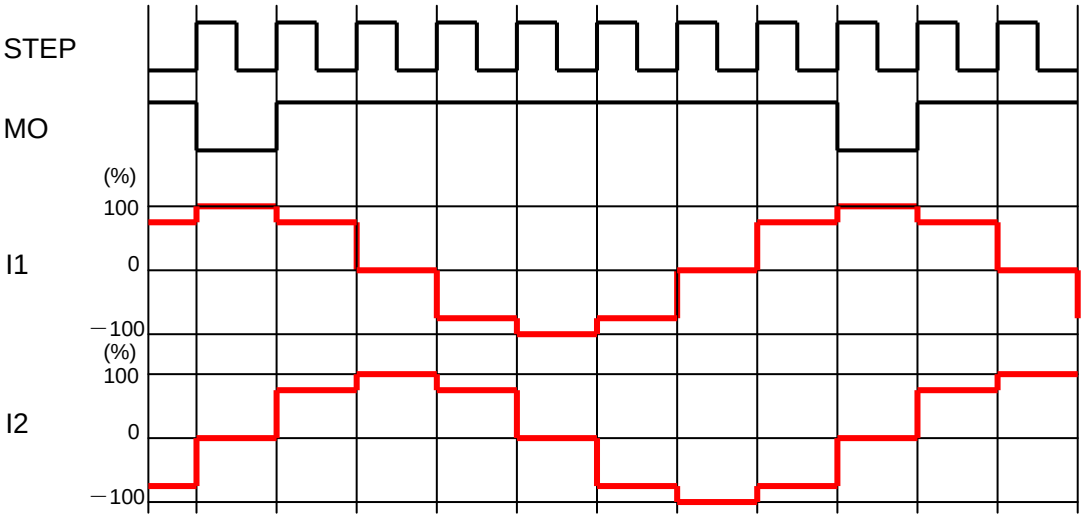
STEP	1/128 (%)		1/64 (%)		1/32 (%)		1/16 (%)		1/8 (%)		Quarter (%)		Half (%)		Full (%)	
	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch	1ch	2ch
θ91	44	90														
θ92	43	90	43	90	43	90										
θ93	42	91														
θ94	41	91	41	91												
θ95	39	92														
θ96	38	92	38	92	38	92	38	92	38	92	38	92				
θ97	37	93														
θ98	36	93	36	93												
θ99	35	94														
θ100	34	94	34	94	34	94										
θ101	33	95														
θ102	31	95	31	95												
θ103	30	95														
θ104	29	96	29	96	29	96	29	96								
θ105	28	96														
θ106	27	96	27	96												
θ107	25	97														
θ108	24	97	24	97	24	97										
θ109	23	97														
θ110	22	98	22	98												
θ111	21	98														
θ112	20	98	20	98	20	98	20	98	20	98						
θ113	18	98														
θ114	17	99	17	99												
θ115	16	99														
θ116	15	99	15	99	15	99										
θ117	13	99														
θ118	12	99	12	99												
θ119	11	99														
θ120	10	100	10	100	10	100	10	100								
θ121	9	100														
θ122	7	100	7	100												
θ123	6	100														
θ124	5	100	5	100	5	100										
θ125	4	100														
θ126	2	100	2	100												
θ127	1	100														
θ128	0	100	0	100	0	100	0	100	0	100	0	100	0	100		

(14) Current wave example in each micro step resolution.

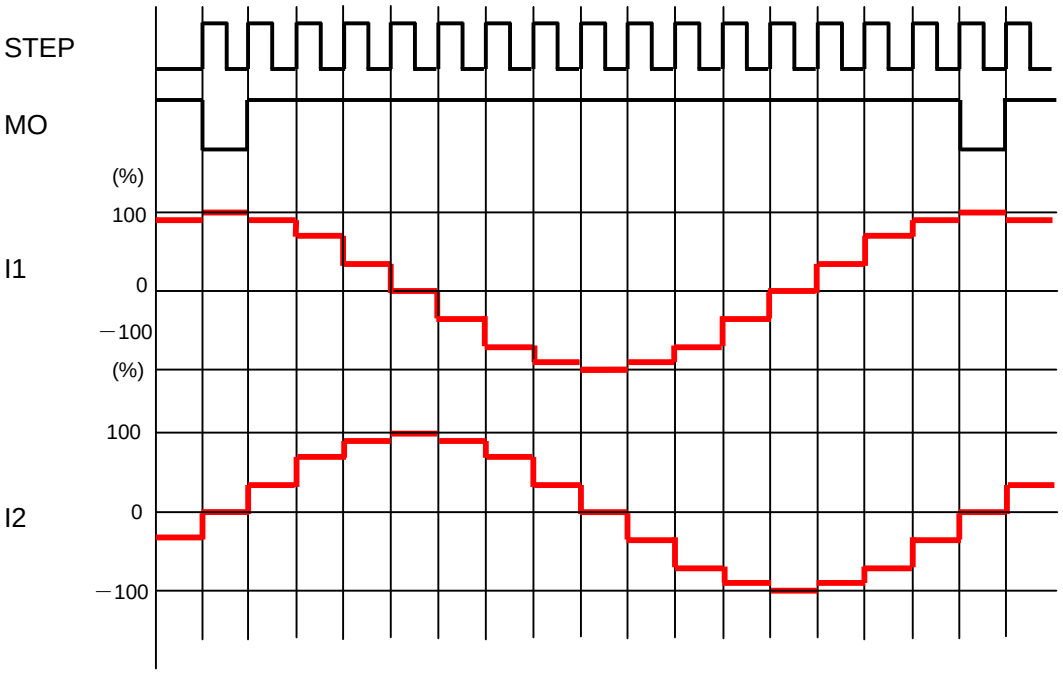
Full Step (CW)



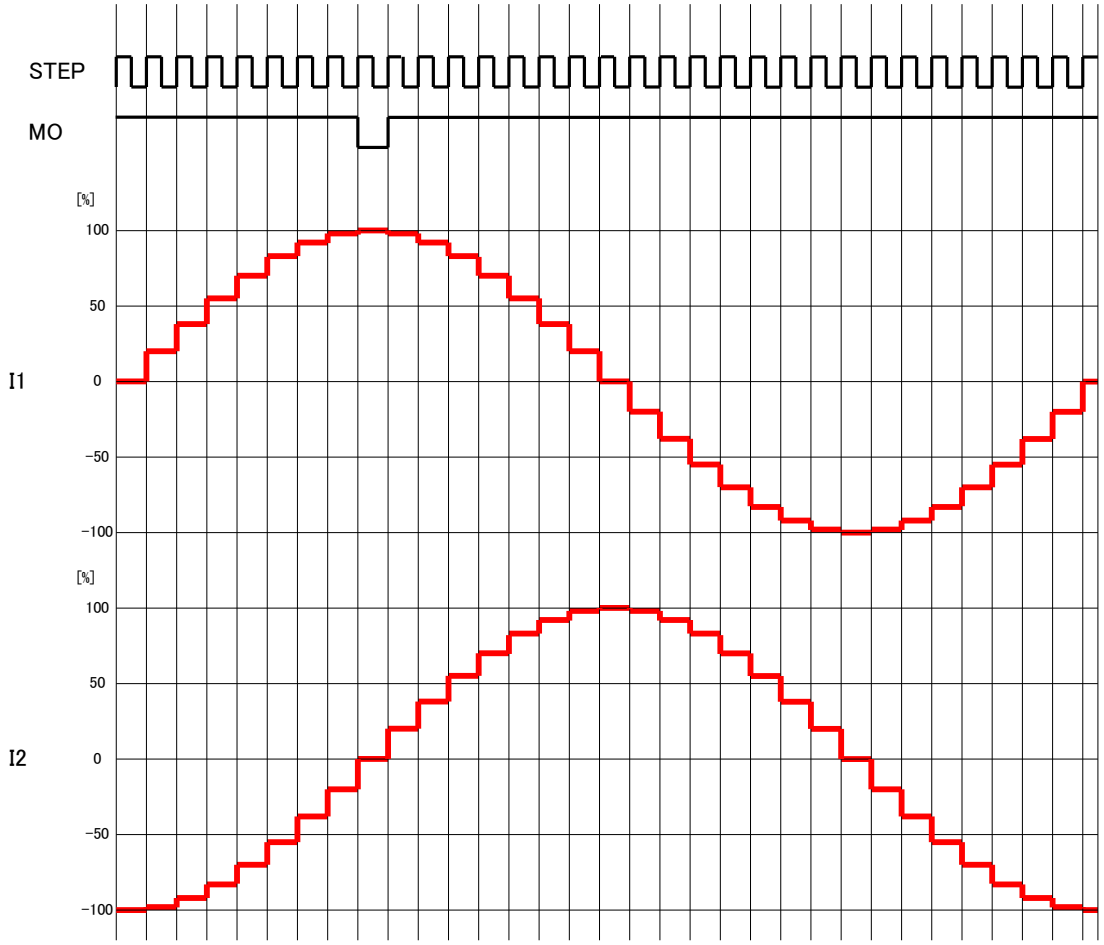
Half Step (CW)



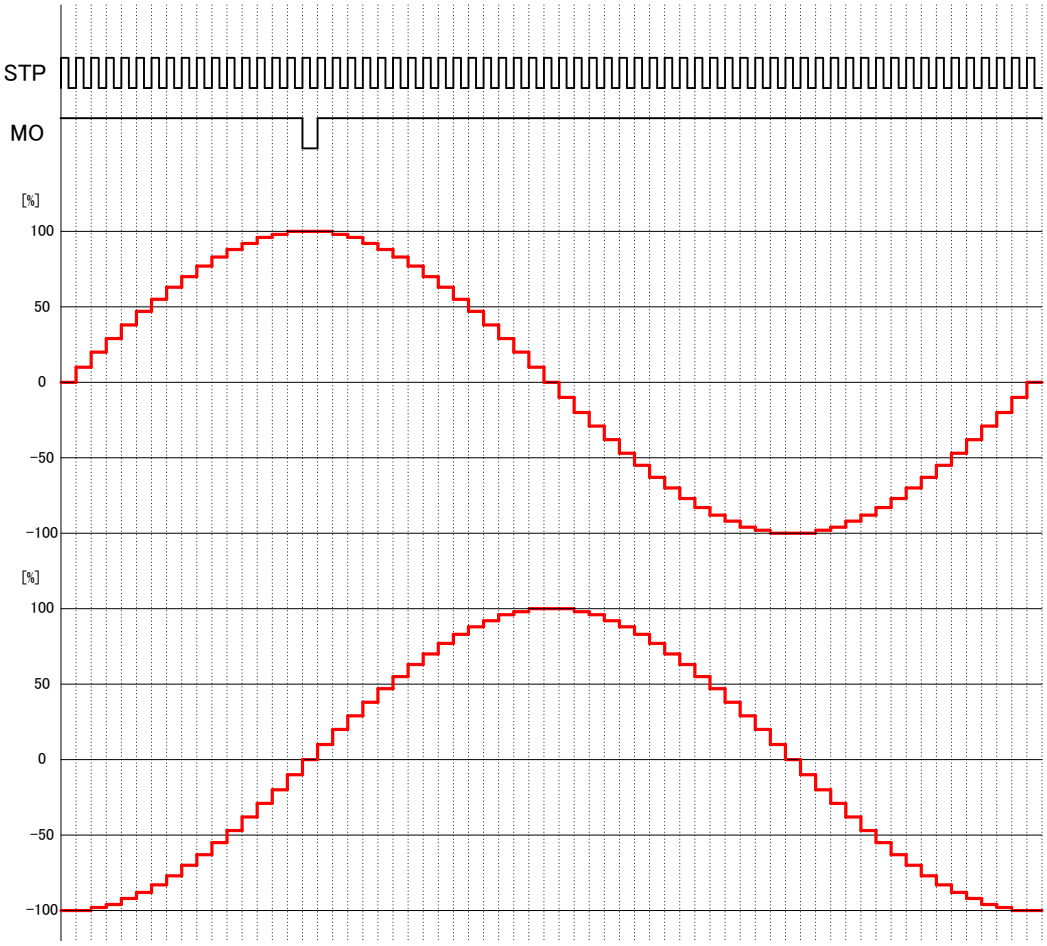
Quarter Step (CW)



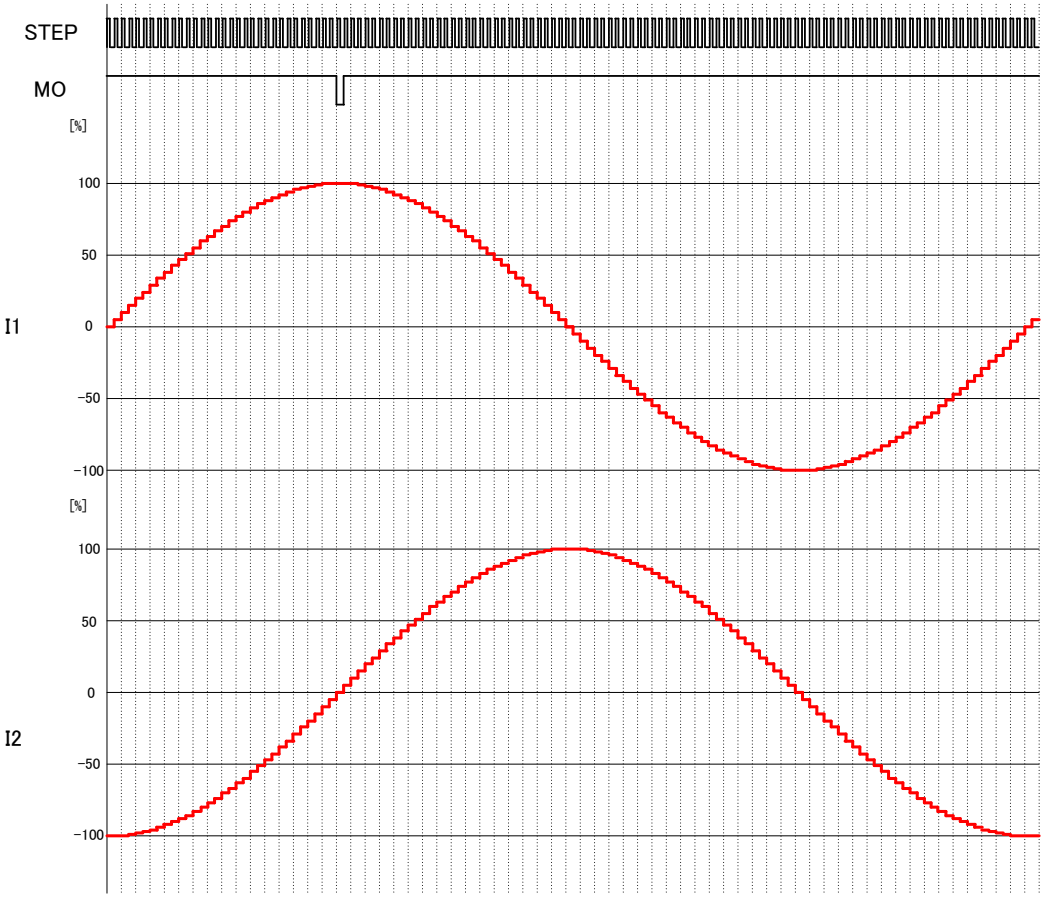
1/8 Step (CW)



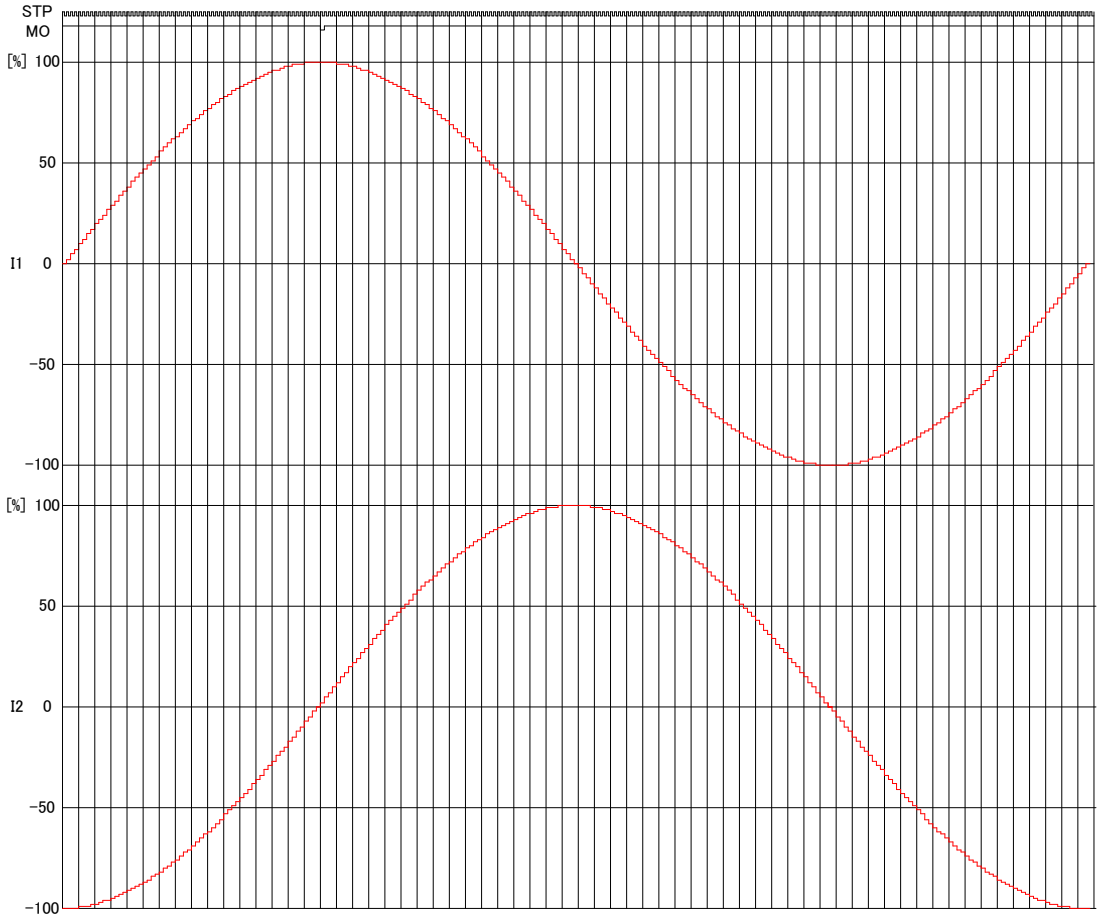
1/16 Step Mode (CW)



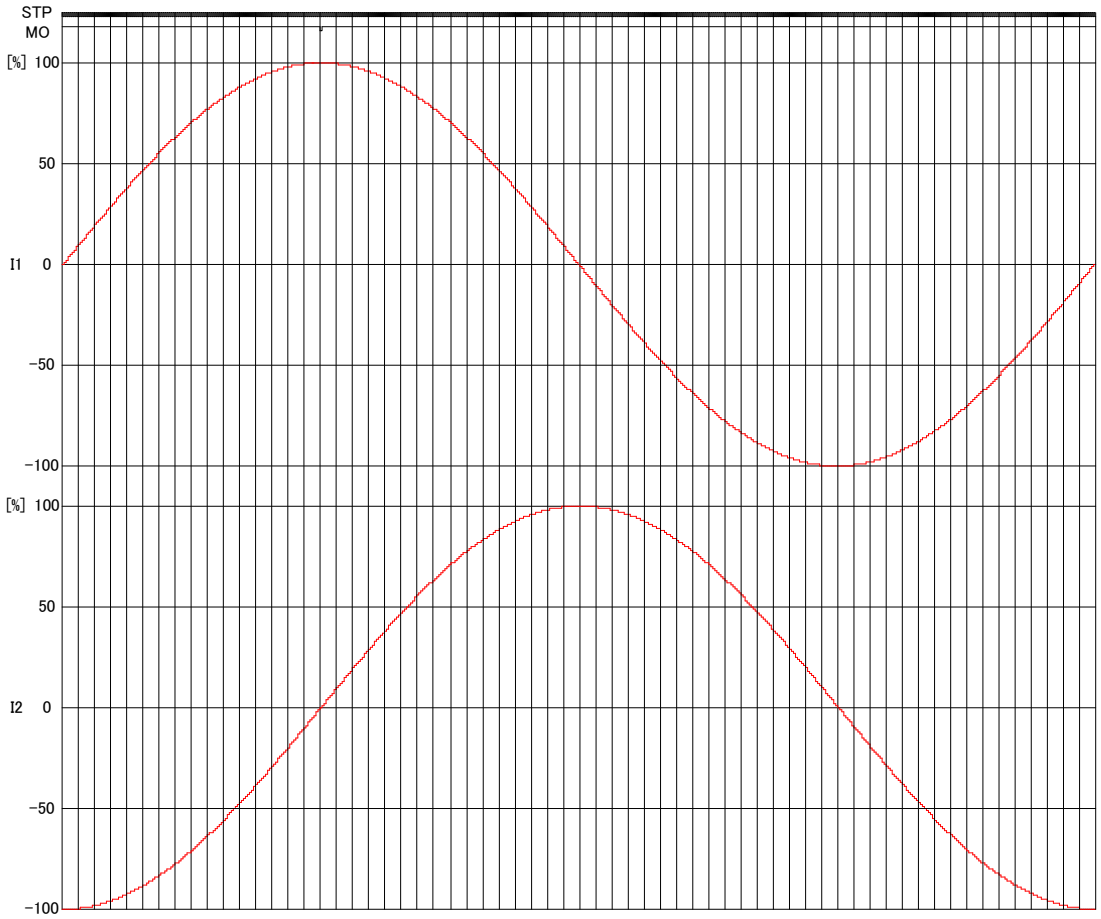
1/32 Step Mode (CW)



1/64 Step Mode (CW)

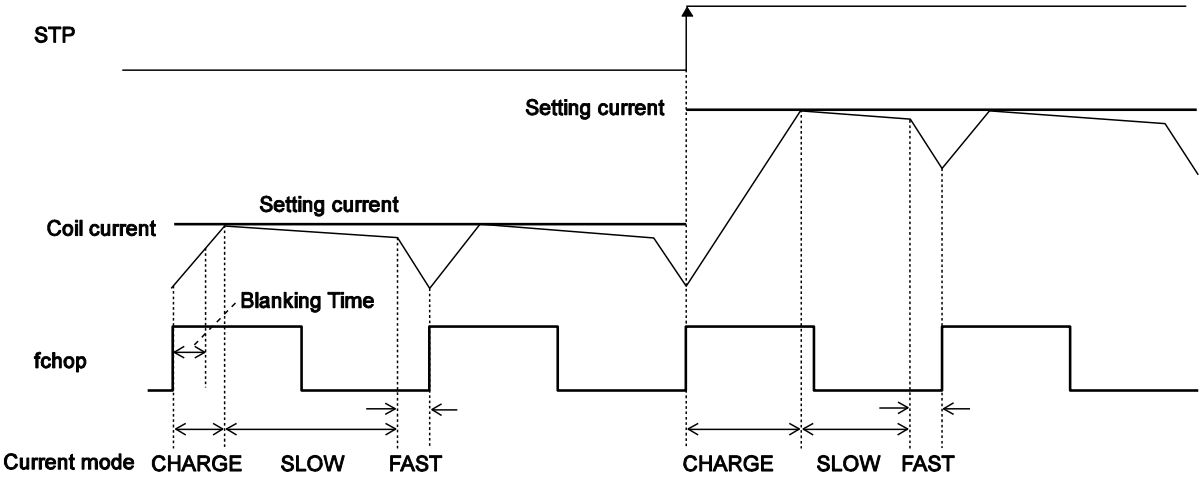


1/128 Step Mode (CW)



(15) Current control operation

(Sine-wave increasing direction)



(Sine-wave decreasing direction)

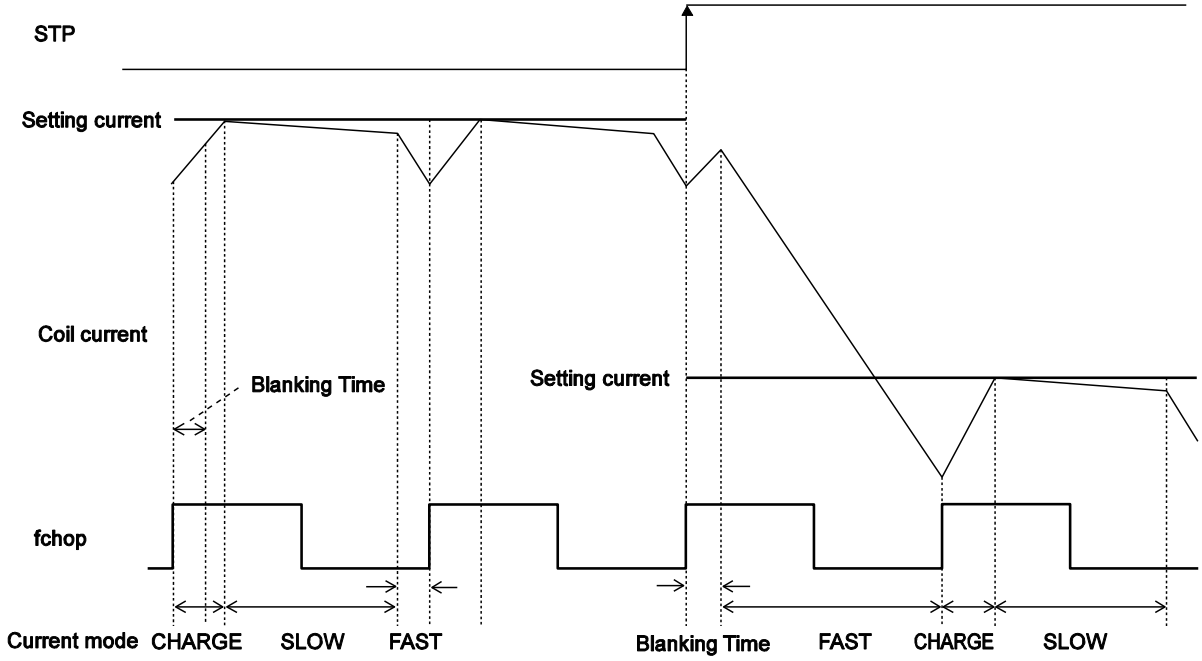


Figure 16. Constant current control timing chart

Each of current modes operates with the follow sequence.

· The IC enters CHARGE mode at a rising edge of the chopping oscillation. (A period of CHARGE mode (Blanking Time) is forcibly present in approximately 1μs, regardless of the current value of the coil current (ICOIL) and set current (IREF)).

· In a period of Blanking Time, the coil current (ICOIL) and the setting current (IREF) are compared.

If an ICOIL < IREF state exists during the charge period:

The IC operates in CHARGE mode until ICOIL ≥ IREF. After that, it switches to SLOW DECAY mode and then switches to FAST DECAY mode in the last approximately 1μs of the period.

If no ICOIL < IREF state exists during the charge period:

The IC switches to FAST DECAY mode and the coil current is attenuated with the FAST DECAY operation until the end of a chopping period.

The above operation is repeated. Normally, in the sine wave increasing direction the IC operates in SLOW (+ FAST) DECAY mode, and in the sine wave decreasing direction the IC operates in FAST DECAY mode until the current is attenuated and reaches the set value and the IC operates in SLOW (+ FAST) DECAY mode.

(16) Output transistor operation mode

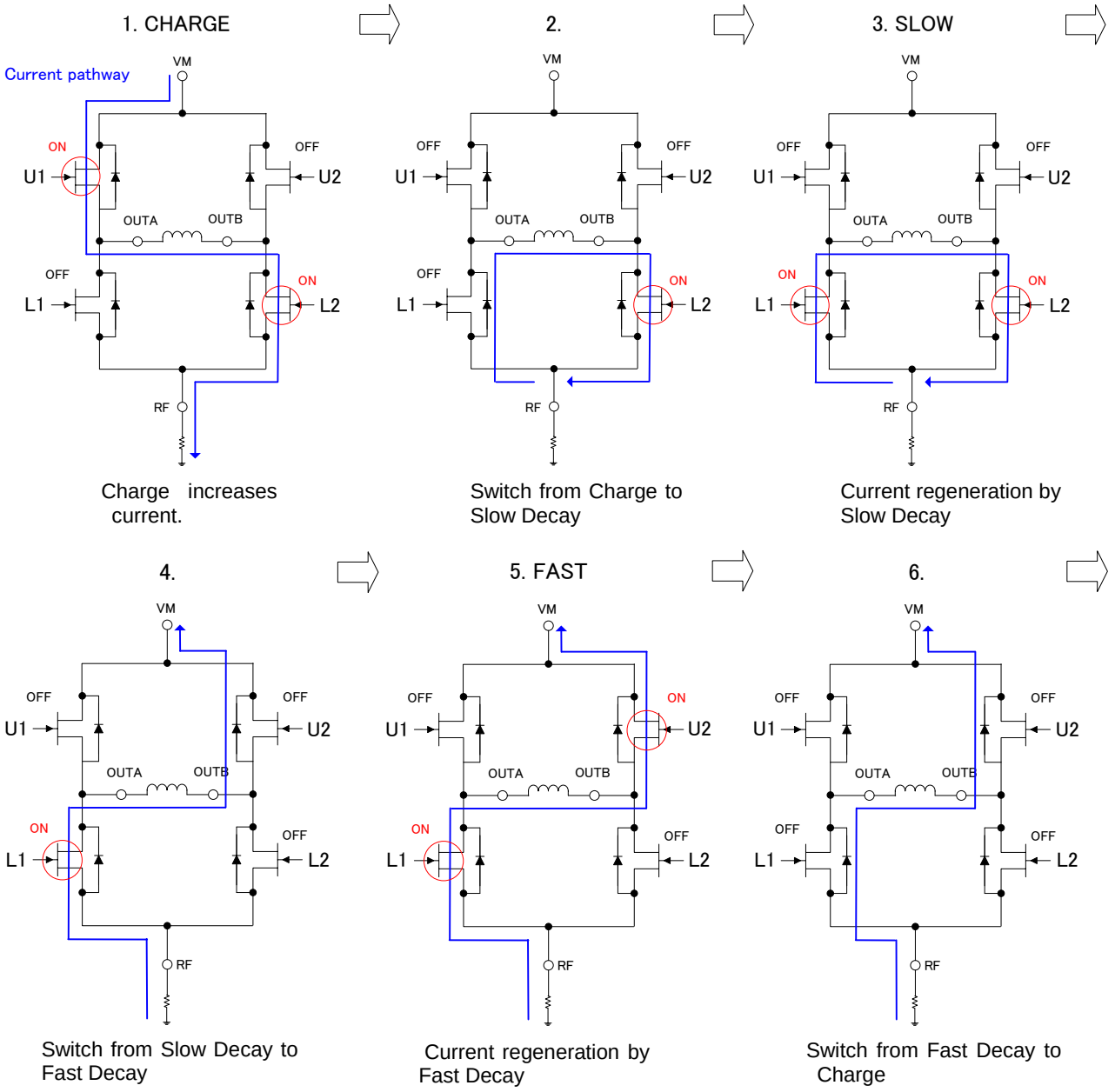


Figure 17. Output transistor operation sequence

This IC controls constant current by performing chopping to output transistor.
As shown above, by repeating the process from 1 to 6, setting current is maintained.
Chopping consists of 3 modes: Charge/ Slow decay/ Fast decay. In this IC, for switching mode (No.2, 4, 6), there are “off period” in upper and lower transistor to prevent crossover current between the transistors. This off period is set to be constant (≈ 0.375μs) which is controlled by the internal logic. The diagrams show parasitic diode generated due to structure of MOS transistor. When the transistor is off, output current is regenerated through this parasitic diode.

Output Transistor Operation Function

OUTA→OUTB (CHARGE)

Output Tr	**CHARGE**	**SLOW**	**FAST**
U1	ON	OFF	OFF
U2	OFF	OFF	ON
L1	OFF	ON	ON
L2	ON	ON	OFF

OUTB→OUTA (CHARGE)

Output Tr	**CHARGE**	**SLOW**	**FAST**
U1	OFF	OFF	ON
U2	ON	OFF	OFF
L1	ON	ON	OFF
L2	OFF	ON	ON

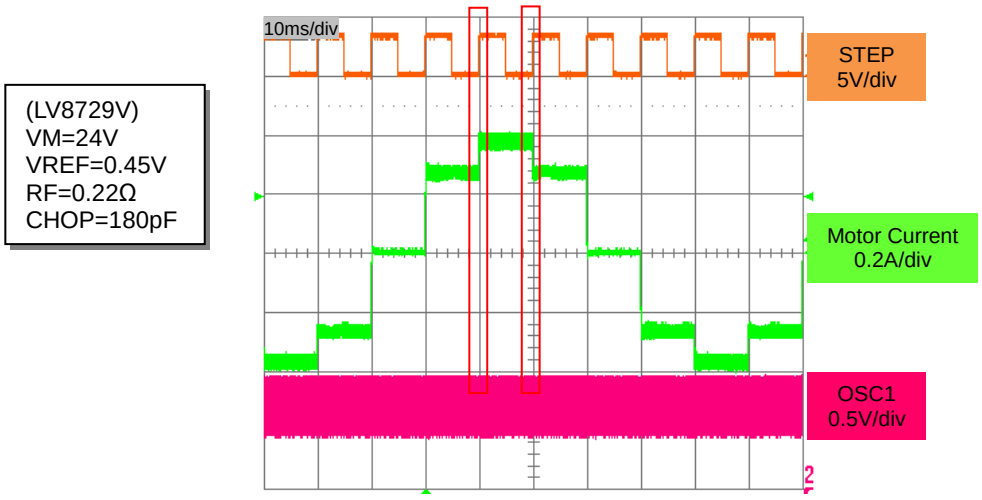


Figure 18.Constant current control waveform

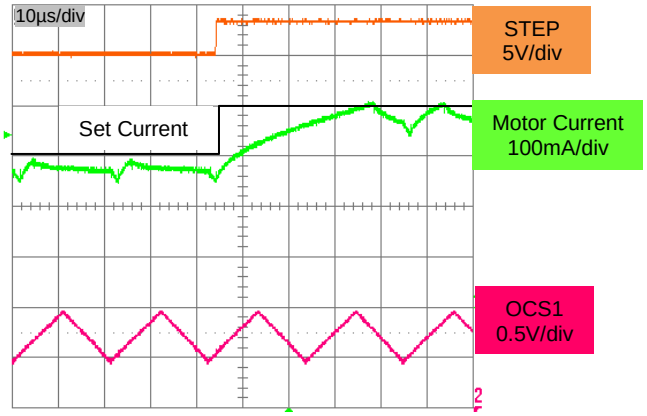


Figure 19. Sine wave increasing direction

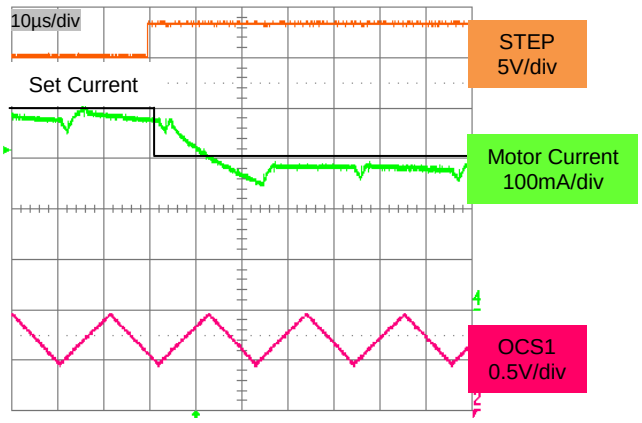
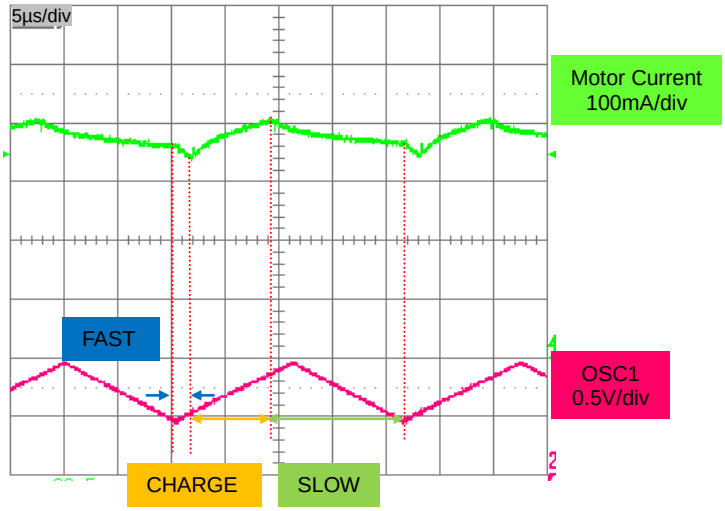


Figure 20. Sine wave decreasing direction

Figure 21. Constant current control waveform (Stationary state)



Motor current switches to Fast Decay mode when triangle wave (CHOP) switches from Discharge to Charge. Approximately after 1µs, the motor current switches to Charge mode. When the current reaches to the setting current, it is switched to Slow Decay mode which continues over the Discharge period of triangle wave.

(17) Blanking period

If, when exercising PWM constant-current chopping control over the motor current, the mode is switched from decay to charge, the recovery current of the parasitic diode may flow to the current sensing resistance, causing noise to be carried on the current sensing resistance pin, and this may result in erroneous detection. To prevent this erroneous detection, a blanking period is provided to prevent the noise occurring during mode switching from being received. During this period, the mode is not switched from charge to decay even if noise is carried on the current sensing resistance pin.
It is approximately 1μs in the blanking time for this IC.

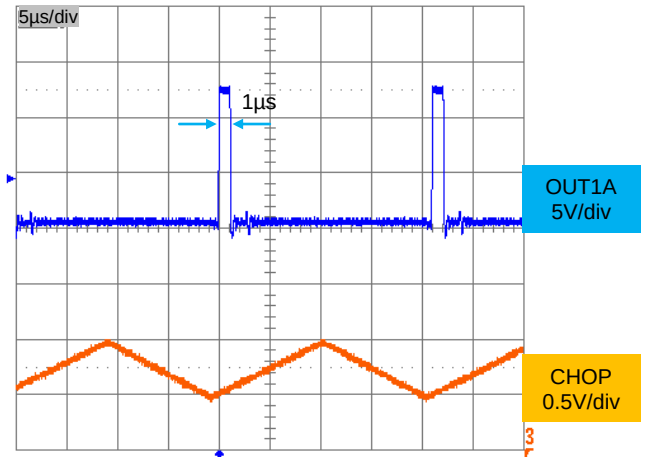


Figure 22.Blanking time waveform

(18) Micro step mode switching operation

When Micro step mode is switched while the motor is rotating, each drive mode operates with the following sequence.

If you switch Microstepping mode while the motor is driving, the mode setting will be reflected from the next STEP and the motor advances to the position shown in the following.

1. Microstepping (1/128-, 1/64-, 1/32-,1/16-,1/8-,Quarter-.Half-step)
→ Microstepping（1/128-, 1/64-, 1/32-,1/16-,1/8-,Quarter-.Half-step）
When a microstepping switches to the next microstepping, the excitation position is switched to the next corresponding step angle of the next microstepping mode.

e.g.) When the rotation direction is forward at 1/8-step, and if you switch to 1/128-step (θ16 - θ47), the step angle is set to θ48 at the next step.
When the rotation direction is forward at 1/128 step. If you switch to 1/8-step (θ48), the step angle is set to θ49 at the next step.

2. Microstepping (1/128-, 1/64-, 1/32-,1/16-,1/8-,Quarter-.Half-step) → Full-step
When a microstepping switches to the full-step, the excitation position is switched to full-step angle of the present quadrant. Caution is required when switching from θ64 or higher step angle of microstepping position to full-step.

e.g.) When the rotation direction is forward at 1/16 step (θ0 - θ124) and if you switch to full-step, the step angle is set to θ64’ at the next step.
When the rotation direction is forward at 1/16 step (θ128) and if you switch to full-step, the step angle is set to -θ64’ at the next step.

3. Full-step → Micro step (1/128-, 1/64-, 1/32-,1/16-,1/8-,Quarter-.Half-step)
When full step switches to microstepping, the excitation position is switched to the next corresponding step angle.

e.g.) When the rotation direction is forward at Full step (θ64’) and if you switch to Quarter-step, the step angle is set toθ96 at the next step.

(Please refer to the step angle on p.13-15 for the description on “θ*”.)

Micro step mode switching operation

● Micro step → Micro step
VM=24V , VDD=5V
VREF=1.1V , RNF=0.22Ω
PS=High , OE=High , RST=High , fSTEP=400Hz

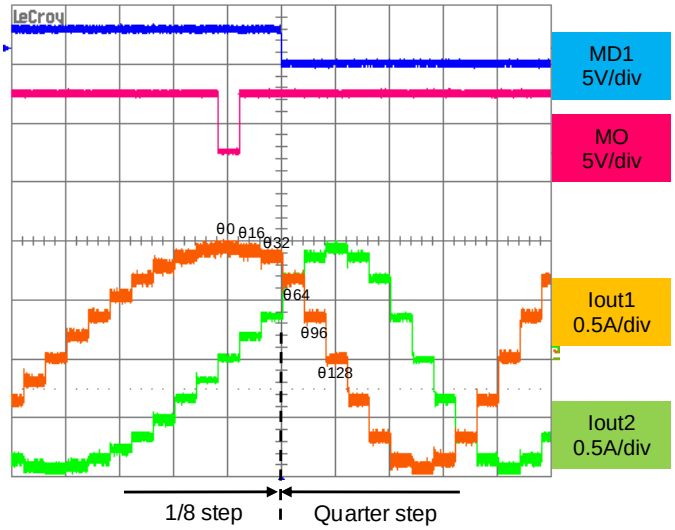


Figure.23 Micro step(1/8step) → Micro step(quarter step)
MD2=High , MD3=Low

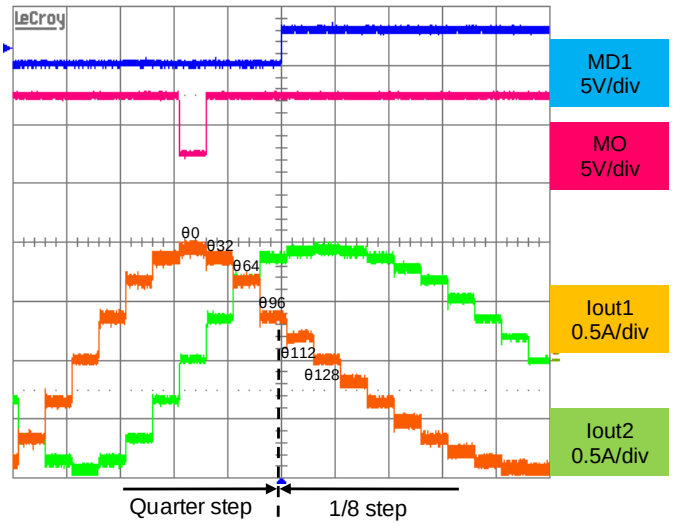


Figure24. Micro step(quarter step) → Micro step(1/8step)
MD2=High , MD3=Low

● Micro step → Full step , Full step → Micro step
VM=24V , VDD=5V
VREF=1.1V , RNF=0.22Ω
PS=High , OE=High , RST=High , fSTEP=200Hz

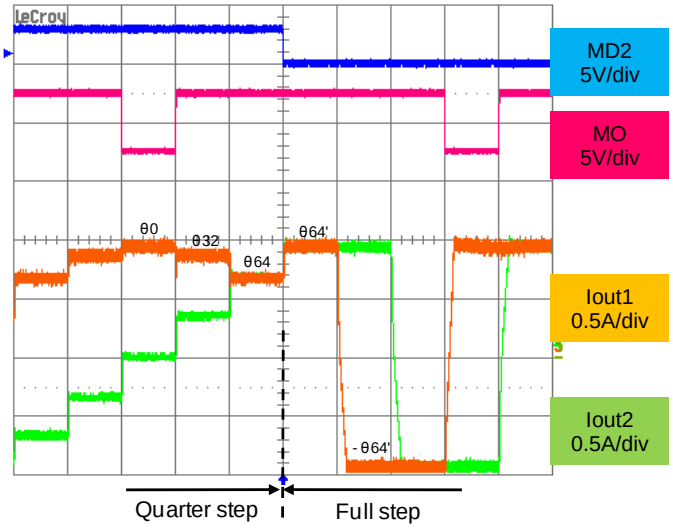


Figure.25 Micro step(quarter step) → Full step
MD1=Low , MD3=Low

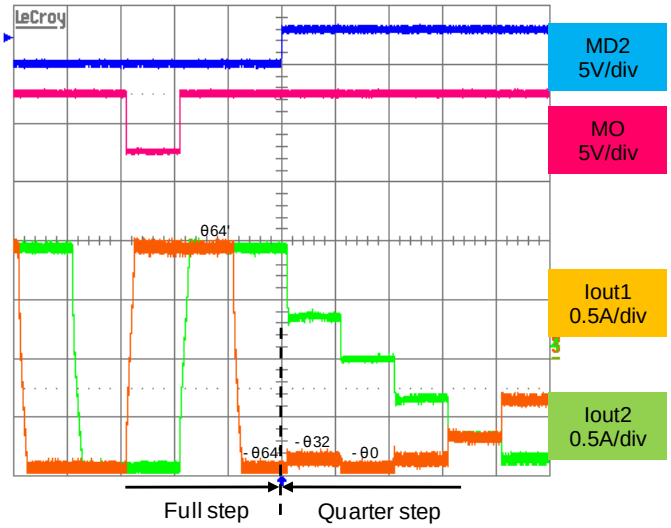
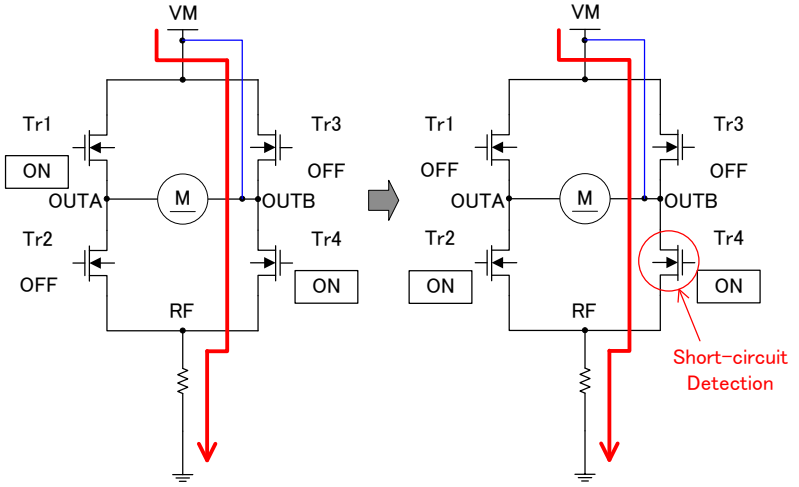


Figure26. Full step → Micro step (quarter step)
MD1=Low , MD3=Low

Output short-circuit protection function

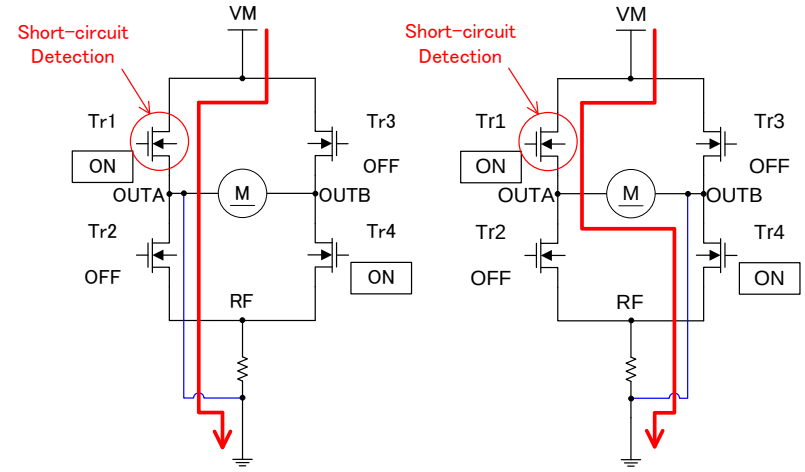
(1) Output short-circuit detection operation

VM short



1.High current flows if Tr3 and Tr4 are ON.
2.If RF voltage> setting voltage, then the mode switches to SLOW decay.
3.If the voltage between D and S of Tr4 exceeds the reference voltage for 2μs, short status is detected.

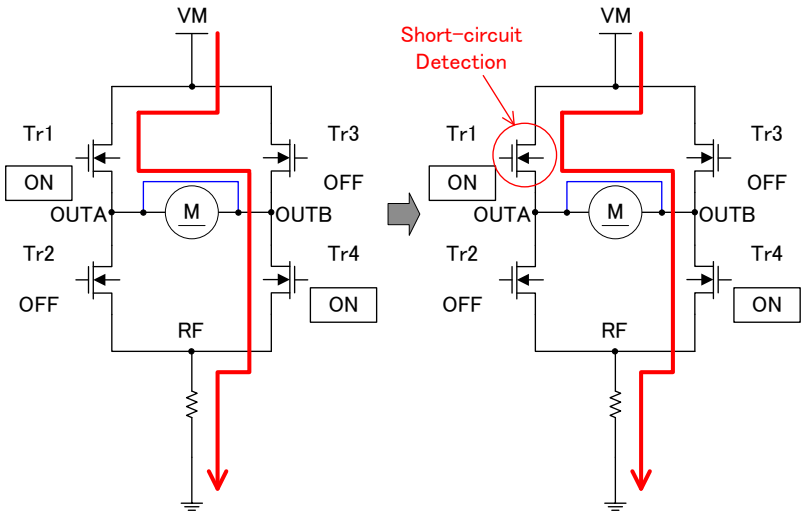
GND short



(left schematic)
1.High current flows if Tr3 and Tr4 are ON
2. If the voltage between D and S of Tr1 exceeds the reference voltage for 2μs, short status is detected.

(right schematic)
1.Without going through RF resistor, current control does not operate and current will continue to increase in CHARGE mode.
2. If the voltage between D and S of Tr1 exceeds the reference voltage for 2μs, short status is detected.

Load short



1.Without L load, high current flows.
2. If RF voltage> setting voltage, then the mode switches to SLOW decay.
3.During load short state in SLOW decay mode, current does not flow and over current state is not detected. Then the mode is switched to FAST decay according to chopping cycle.
4. Since FAST state is short (≈1μs), switches to CHARGE mode before short is detected.
5.If voltage between D and S exceeds the reference voltage continuously during blanking time at the start of CHARGE mode (Tr1), CHARGE state is fixed (even if RF voltage exceeds the setting voltage, the mode is not switched to SLOW decay). After 2us or so, short is detected.

(2) Output short-circuit protection detect current (Reference value)

Short protector operates when abnormal current flows into the output transistor.

Ta = 25°C (typ)

Upper-side Transistor	4.46A
Lower-side Transistor	4.04A

*RF=GND

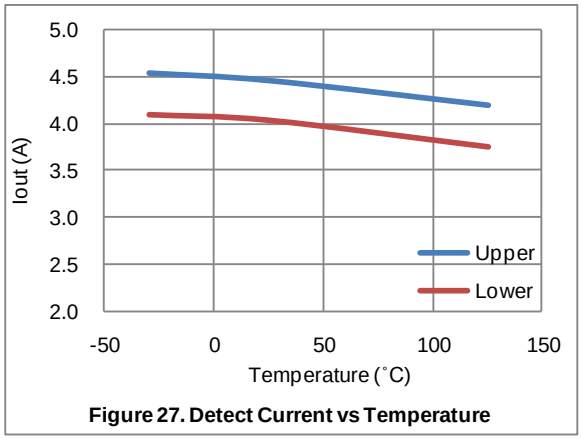


Figure 27. Detect Current vs Temperature

(3) Timer latch period

Built-in output short-circuit protection circuit makes output to enter in stand-by mode. This function prevents the IC from damaging when the output shorts circuit by a voltage short or a ground short, etc. When output short state is detected for 2µs, short-circuit detection circuit state the operating and output is once turned OFF. Subsequently, the output is turned ON again after the timer latch period (typ. 256µs). If the output remains in the short-circuit state, turn OFF the output, fix the output to the wait mode, and turn ON the EMO output. When output is fixed in stand-by mode by output short protection circuit, output is released the latch by setting ST = "L".

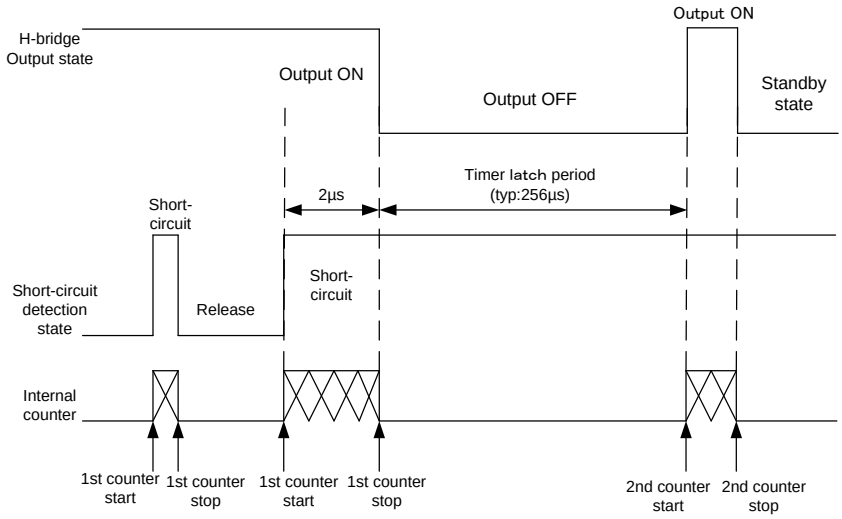


Figure 28 . short-circuit protection function timing chart

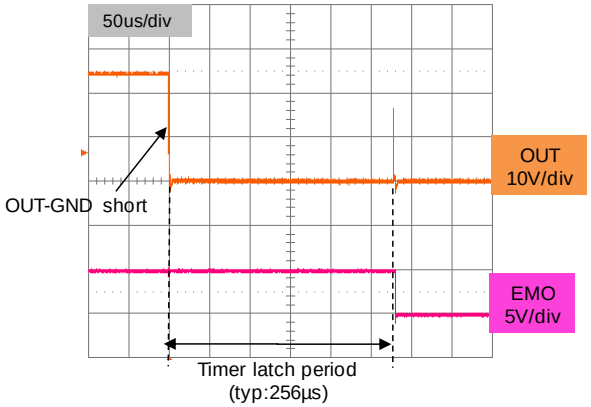


Figure 29. Timer latch period waveform

(4) Unusual condition warning output pins (EMO)

The LV8729V is provided with the EMO pin which notifies the CPU of an unusual condition if the protection circuit operates by detecting an unusual condition of the IC. This pin is of the open-drain output type and when an unusual condition is detected, the EMO output is placed in the ON (EMO = Low) state.

Furthermore, the EMO pin is placed in the ON state when one of the following conditions occurs.

1. Shorting-to-power, shorting-to-ground, or shorting-to-load occurs at the output pin and the output short-circuit protection circuit is activated.
2. The IC junction temperature rises and the thermal protection circuit is activated.

Thermal shutdown function

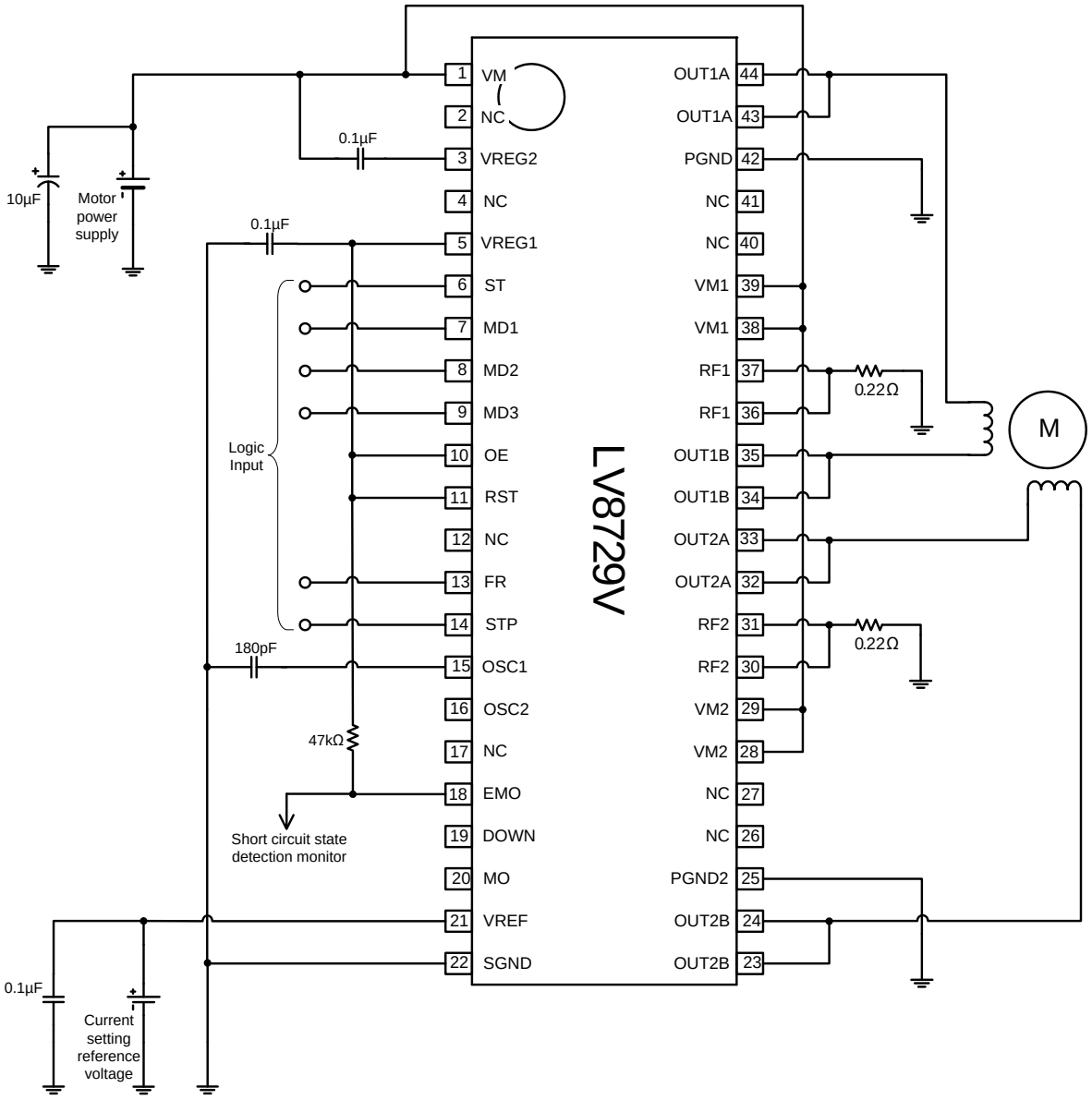
The thermal shutdown circuit is incorporated and the output is turned off when junction temperature Tj exceeds 180°C and the abnormal state warning output is turned on. As the temperature falls by hysteresis, the output turned on again (automatic restoration).

The thermal shutdown circuit does not guarantee the protection of the final product because it operates when the temperature exceed the junction temperature of Tjmax=150°C.

TSD = 180°C (typ)

ΔTSD = 40°C (typ)

Application Circuit Example



The above sample application circuit is set to the following conditions:

- Output enable function fixed to the output state (OE = “H”)
- Reset function fixed to the output state (RST = “H”)
- Chopping frequency : 55.5kHz (Cosc1 = 180pF)

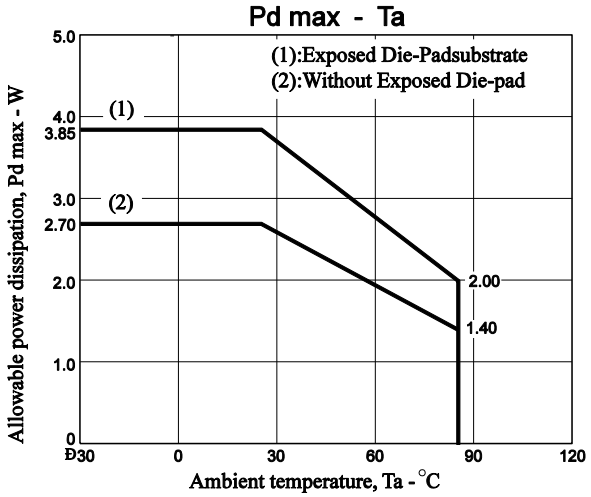
The set current value is as follows :

I_{OUT} = (Current setting reference voltage / 5) / 0.22Ω

Allowable power dissipation

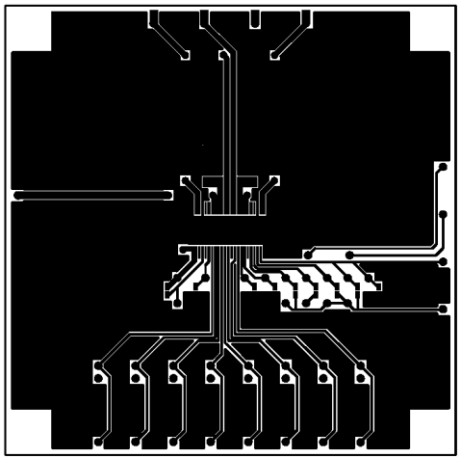
・The pad on the backside of the IC functions as heatsink by soldering with the board. Since the heat-sink characteristics vary depends on board type, wiring and soldering, please perform evaluation with your board for confirmation.

Specified circuit board : 90mm x 90mm x 1.6mm, glass epoxy 2-layer board

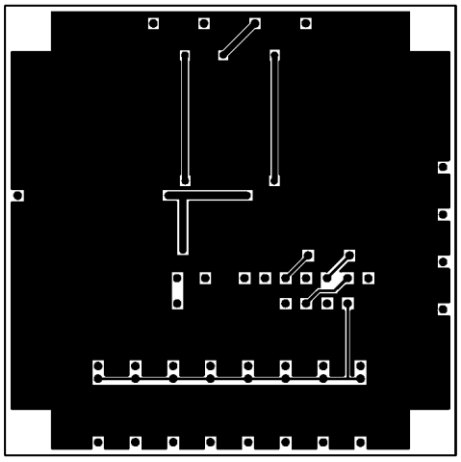


Substrate Specifications (Substrate recommended for operation of LV8729V)

Size : 90mm × 90mm × 1.6mm (two-layer substrate [2S0P])
Material : Glass epoxy
Copper wiring density : L1 = 85% / L2 = 90%



L1 : Copper wiring pattern diagram



L2 : Copper wiring pattern diagram

Cautions

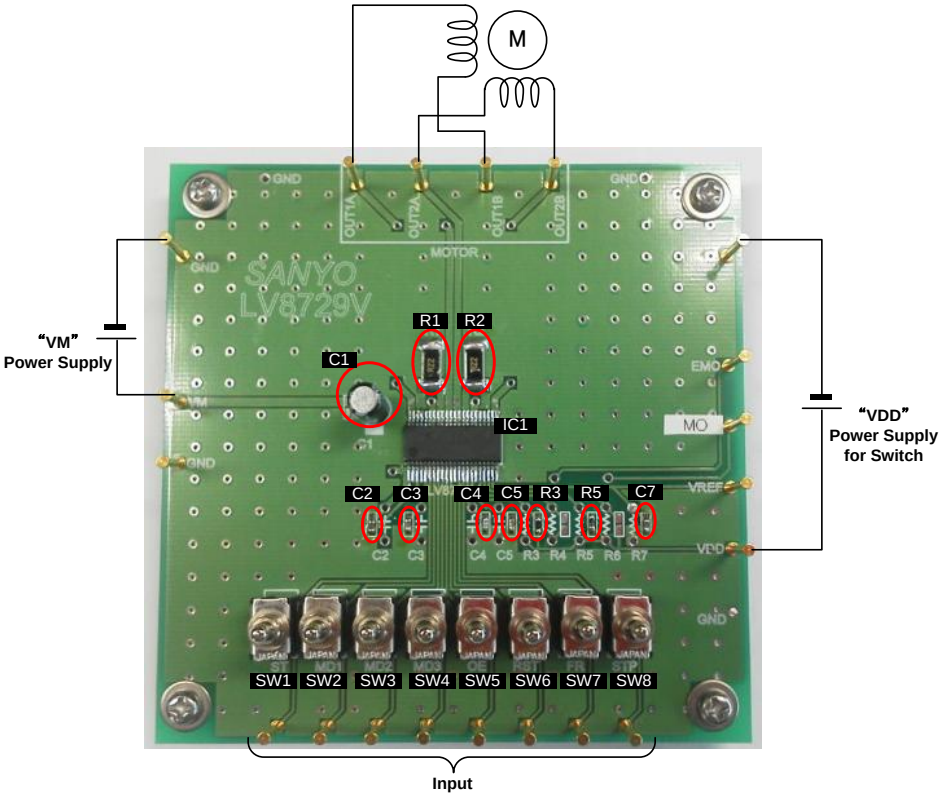
1) The data for the case with the Exposed Die-Pad substrate mounted shows the values when 90% or more of the Exposed Die-Pad is wet.

2) For the set design, employ the derating design with sufficient margin.
Stresses to be derated include the voltage, current, junction temperature, power loss, and mechanical stresses such as vibration, impact, and tension.
Accordingly, the design must ensure these stresses to be as low or small as possible.
The guideline for ordinary derating is shown below :
(1)Maximum value 80% or less for the voltage rating
(2)Maximum value 80% or less for the current rating
(3)Maximum value 80% or less for the temperature rating

3) After the set design, be sure to verify the design with the actual product.
Confirm the solder joint state and verify also the reliability of solder joint for the Exposed Die-Pad, etc.
Any void or deterioration, if observed in the solder joint of these parts, causes deteriorated thermal conduction, possibly resulting in thermal destruction of IC.

Evaluation board

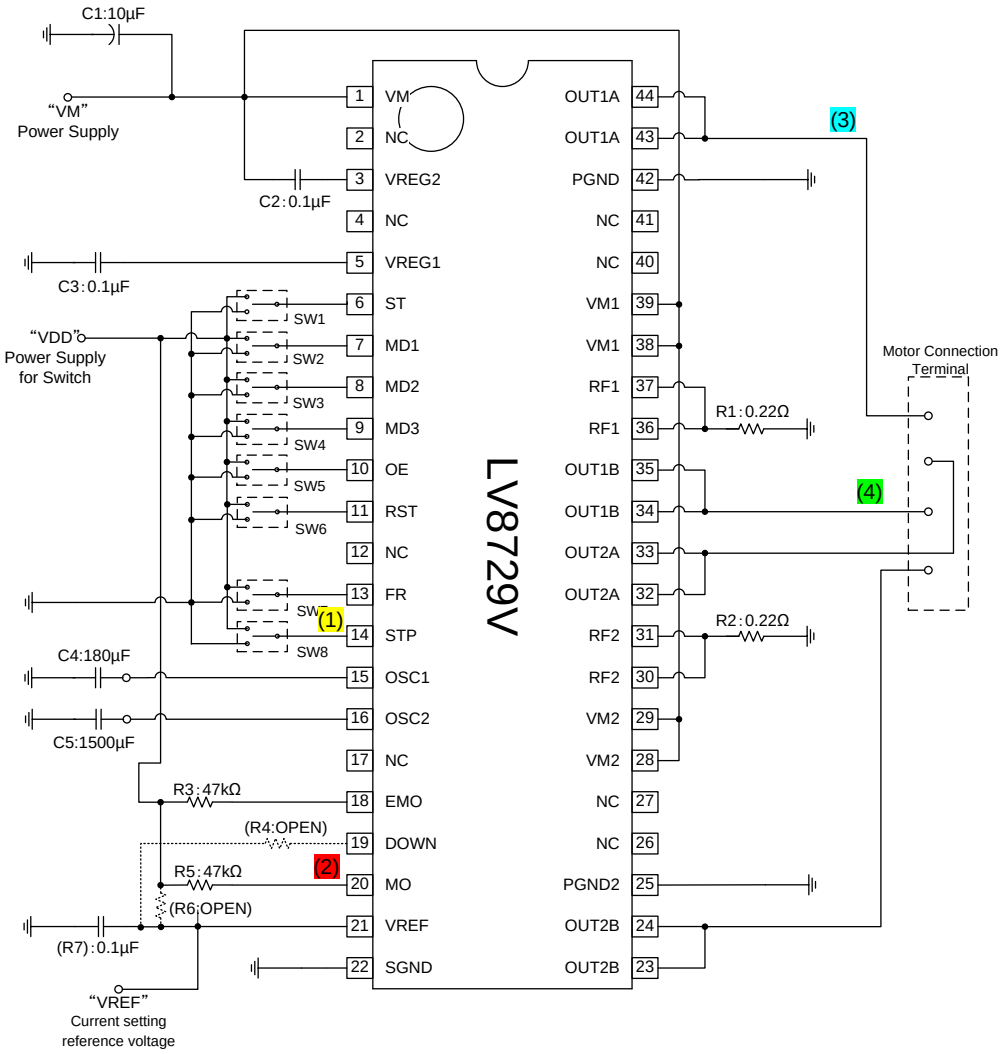
LV8729V (90mm x 90mm x 1.6mm, glass epoxy 2-layer board, with backside mounting)



Bill of Materials for LV8729V Evaluation Board

Designator	Qty	Description	Value	Tol	Footprint	Manufacturer	Manufacturer Part Number	Substitution Allowed	Lead Free
C1	1	VM Bypass capacitor	10µF 50V	±20%		SUN Electronic Industries	50ME10HC	yes	yes
C2	1	VREG2 stabilization Capacitor	0.1µF 100V	±10%		murata	GRM188R72A104KA35D	yes	yes
C3	1	VREG1 stabilization Capacitor	0.1µF 100V	±10%		murata	GRM188R72A104KA35D	yes	yes
C4	1	Capacitor to set chopping frequency	180pF 50V	±5%		murata	GRM1882C1H181JA01	yes	yes
C5	1	Capacitor to set switching holding current	1500pF 50V	±5%		KOA	GRM1882C1H152J	yes	yes
R1	1	Channel 1 Output current detective Resistor	0.22Ω 1W	±5%		ROHM	MCR100JZHJLR22	yes	yes
R2	1	Channel 2 Output current detective Resistor	0.22Ω 1W	±5%		ROHM	MCR100JZHJLR22	yes	yes
R3	1	Pull-up Resistor for terminal EMO	47kΩ 1/10W	±5%		KOA	RK73B1JT473J	yes	yes
R5	1	Pull-up Resistor for terminal MO	47kΩ 1/10W	±5%		KOA	RK73B1JT473J	yes	yes
R7	1	VREF stabilization Capacitor	0.1µF 100V	±10%		murata	GRM188R72A104KA35D	yes	yes
IC1	1	Motor Driver			SSOP44K (275mil)	SANYO semiconductors	LV8729V	No	yes
SW1-SW8	8	Switch				MIYAMA	MS-621-A01	yes	yes
TP1-TP20	20	Test points				MAC8	ST-1-3	yes	yes

Evaluation board circuit



Evaluation Board Manual

[Supply Voltage] VM (9 to 32V): Power Supply for LSI
VREF (0 to 3V): Const. Current Control for Reference Voltage
VDD (2 to 5V): Logic "High" voltage for toggle switch

[Toggle Switch State] Upper Side: High (VDD)
Middle: Open, enable to external logic input
Lower Side: Low (GND)

[Operation Guide]

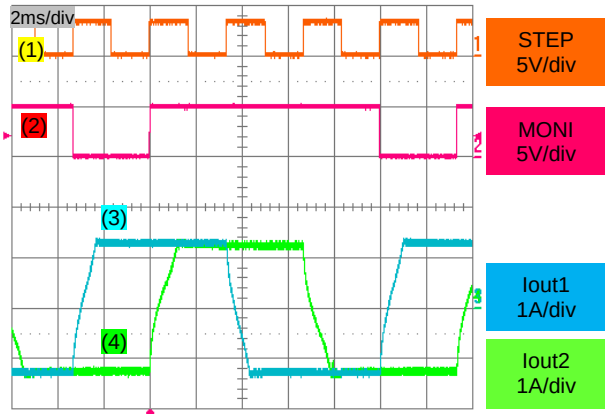
1. **Initial Condition Setting:** Set "Open" the toggle switch STEP, and "Open or Low" the other switches
2. **Motor Connection:** Connect the Motors between OUT1A and OUT1B, between OUT2A and OUT2B.
3. **Power Supply:** Supply DC voltage to VM, VREF and VDD.
4. **Ready for Operation from Standby State:** Turn "High" the following toggle switches : ST , OE, and RST. Channel 1 and 2 are into Full-Step excitement initial position (100%, -100%).
5. **Motor Operation:** Input the clock signal into the terminal STEP.
6. **Other Setting** (See Application Note for detail)
   i. MD1 , MD2 , MD3 : Micro step resolution.
   ii. FR: Motor rotation direction (CW / CCW) setting.
   iii. RST : Initial Mode.
   iv. OE: Output Enable.

[Setting for External Component Value]

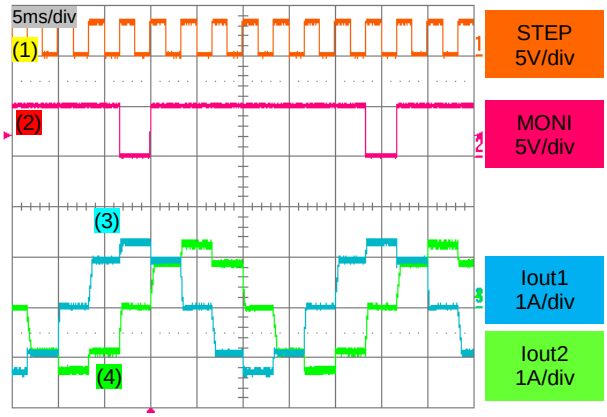
1. Constant Current (100%)
   At VREF=1.5V
   Iout =VREF [V] / 5 / RF [ohm]
   =1.5 [V] / 5 / 0.22 [ohm]
   =1.36 [A]
2. Chopping Frequency
   Fcp = 1 / (Cosc1 / 10 x 10^{-6}) (Hz)
   =1 / (180 [pF] / 10 x 10^{-6}) (Hz)
   =55.5 [kHz]

Waveform of LV8729V evaluation board.

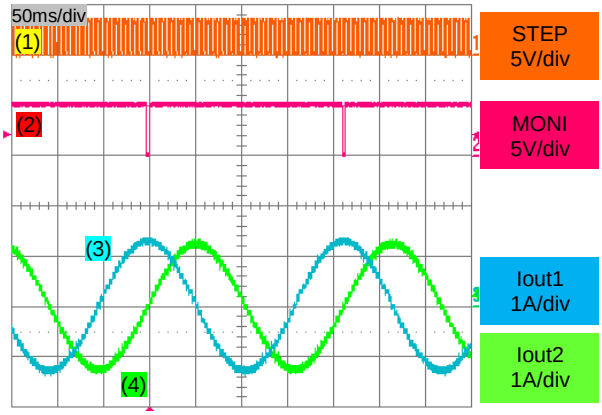
●Figure 30. Full Step
VM=24V , VREF=1.5V , VDD=5V
ST=H , OE=H , RST=H
FR=L
MD1=L , MD2=L , MD3=L
STEP=300Hz (Duty 50%)



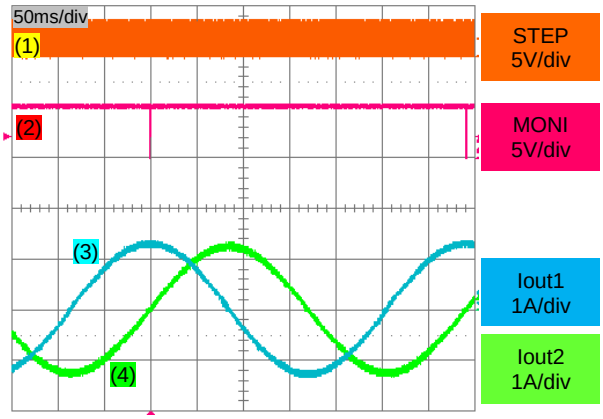
●Figure 31. Half Step
VM=24V , VREF=1.5V , VDD=5V
ST=H , OE=H , RST=H
FR=L
MD1=H , MD2=L , MD3=L
STEP=300Hz (Duty 50%)



●Figure 32. 1/16 Step
VM=24V , VREF=1.5V , VDD=5V
ST=H , OE=H , RST=H
FR=L
MD1=L , MD2=L , MD3=H
STEP=300Hz (Duty 50%)



●Figure 33. 1/128 Step
VM=24V , VREF=1.5V , VDD=5V
ST=H , OE=H , RST=H
FR=L
MD1=H , MD2=H , MD3=H
STEP=1500Hz (Duty 50%)



Warning:

●Power supply connection terminal【VM, VM1, VM2】

- ✓ Make sure to short-circuit VM, VM1 and VM2.For controller supply voltage, the internal regulator voltage of VREG1 (typ 5V) is used.
- ✓ Make sure that supply voltage does not exceed the absolute MAX ratings under no circumstance. Noncompliance can be the cause of IC destruction and degradation.
- ✓ Caution is required for supply voltage because this IC performs switching.
- ✓ The bypass capacitor of the power supply should be close to the IC as much as possible to stabilize voltage. Also if you intend to use high current or back EMF is high, please augment enough capacitance.

●GND terminal【GND, PGND, Exposed Die-Pad】

- ✓ Since GND is the reference of the IC internal operation, make sure to connect to stable and the lowest possible potential. Since high current flows into PGND, connect it to one-point GND.
- ✓ The exposed die-pad is connected to the board frame of the IC. Therefore, do not connect it other than GND. Independent layout is preferable. If such layout is not feasible, please connect it to signal GND. Or if the area of GND and PGND is larger, you may connect the exposed die pad to the GND.

(The independent connection of exposed die pad to PGND is not recommended.)

●Internal power supply regulator terminal【VREG1】

- ✓ VREG1 is the power supply for logic (typ 5V).
- ✓ When VM supply is powered and ST is ”H”, VREG1 operates.
- ✓ Please connect capacitor for stabilize VREG1. The recommendation value is 0.1μF.
- ✓ Since the voltage of VREG1 fluctuates, do not use it as reference voltage that requires accuracy.

●Input terminal

- ✓ The logic input pin incorporates pull-down resistor (100kΩ).
- ✓ When you set input pin to low voltage, please short it to GND because the input pin is vulnerable to noise.
- ✓ The input is TTL level (H: 2V or higher, L: 0.8V or lower).
- ✓ VREF pin is high impedance.

●OUT terminal【OUT1A, OUT1B, OUT2A, OUT2B】

- ✓ During chopping operation, the output voltage becomes equivalent to VM voltage, which can be the cause of noise. Caution is required for the pattern layout of output pin.
- ✓ The layout should be low impedance because driving current of motor flows into the output pin.
- ✓ Output voltage may boost due to back EMF. Make sure that the voltage does not exceed the absolute MAX ratings under no circumstance. Noncompliance can be the cause of IC destruction and degradation.

●Current sense resistor connection terminal【RF1, RF2】

- ✓ To perform constant current control, please connect resistor to RF pin.
- ✓ To perform saturation drive (without constant current control), please connect RF pin to GND.
- ✓ If RF pin is open, then short protector circuit operates. Therefore, please connect it to resistor or GND.
- ✓ The motor current flows into RF – GND line. Therefore, please connect it to common GND line and low impedance line.

●NC terminal

- ✓ NC pin is not connected to the IC.
- ✓ If VM line and output line are wide enough in your layout, please use NC.

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